# GT25D20/10/05E

## 2M/1M/512K Bits
## SPI Nor Flash

## Contents

## 1. Features

- Single Power Supply Voltage
  - Full voltage range: 1.65~3.6V
- Operating Temperature range:
  - –40 to +85 °C
  - –40 to +105 °C
- 2M/1M/512K-bit Serial Flash
  - 256K/128K/64K-byte
  - 256 bytes per programmable page
- Standard, Dual SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, IO0, IO1, WP#
- High Speed Clock Frequency
  - 104MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 208Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top Block protection
- Allows XIP (execute in place) Operation
  - Continuous Read With 8/16/32/64-byte Wrap
- Data Retention
  - 20-year data retention typical
- Minimum 100,000 Program/Erase Cycles
- ESD protection (Human Body Model)
  - –4000V to +4000V
- Fast Program/Erase Speed
  - Page Program time: 1.25ms typical
  - Sector Erase time: 2.5ms typical
  - Block Erase time: 2.5ms typical
  - Chip Erase time: 5ms typical
- Flexible Architecture
  - Uniform Sector of 4K-byte
  - Uniform Block of 32/64K-byte
- Low Power Consumption
  - 7uA typical Standby current
  - 0.1uA typical power down current
- Advanced security Features
  - 64-Bit Unique Serial Number for each device
- Space Efficient Packaging:
  - 8-pin SOIC 208/150 mil
  - 8-pad WSON 6X5 mm
  - 8-pad USON8 2X3 mm
  - 8-pin TSSOP
  - 8-Land USON 1.5*1.5mm
  - 6-Land USON 1.2*1.2mm
  - 6-Land USON 0.72*1.0mm
  - 6-Land USON 0.72*1.1mm
  - Contact Giantec for KGD and other

## 2. Genera Description

GT25D20/10/05E is 2Mb/1Mb/512Kb bits Serial NOR Flash, the array is organized into 1024 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB Sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase), The device operates on a single 1.65V to 3.6V power supply with current consumption as low as 1uA Standby current and 0.1μA for power-down. All devices are offered in space-saving packages.

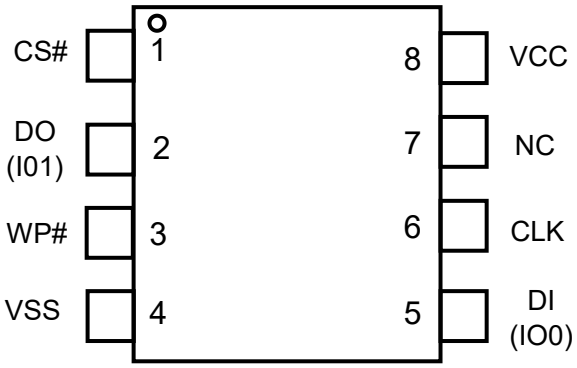
The GT25D20/10/05E supports the standard Serial Peripheral Interface (SPI), and a high performance Dual output as well as Dual I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O when using the Fast Read Dual I/O instructions.

A Write Protect pin and programmable write protection, with top,bottom or complement array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique ID. GT25D20/10/05E features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (CLK), a serial data input (DI), and a serial data output (DO). Serial access to the device is enabled by CS# input.

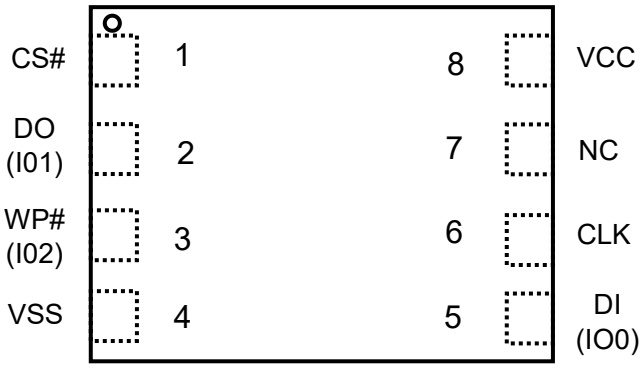
## 3.Package Types:

GT25D20/10/05E is offered in an 8-pin plastic 208mil/150-mil width SOIC (package code W/G),an 8-pad WSON 6X5-mm (package code WS) ,an 8-pad USON 2x3-mm (package code ED), an 8-pin TSSOP (package code Z) and 6-Land USON 0.72x1.0 as below.Package diagrams and dimensions are illustrated at the end of this datasheet.

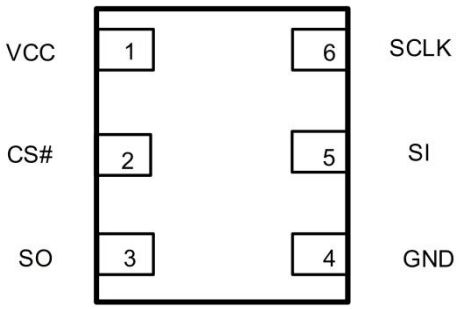
### 3.1 Pin Configuration




SOP8 208mil/150mil and TSSOP




WSON 8x6 / USON 2x3/ USON 1.5x1.5




6-Land USON 1.2x1.2/0.72x1.0/0.72x1.1

## 3.2 Pin Description

| Pin Name | I/O | Function |
|---|---|---|
| /CS | I | Chip Select Input |
| DO(IO1) | I/O | Data Output (Data Input Output 1)*1 |
| /WP | I/O | Write Protect Input |
| GND | | Ground |
| DI(I/O0) | I/O | Data Input (Data Input Output 0)*1 |
| CLK | I | Serial Clock Input |
| NC | NC | No Connection |
| VCC | | Power Supply |

## 3.3 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device.After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection”). If needed a pull-up resister on /CS can be used to accomplish this.

## 3.4 Serial Data Input, Output and IOs (DI, DO and IO0, IO1)

The GT25D20/10/05E supports standard SPI, Dual SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

## 3.5 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

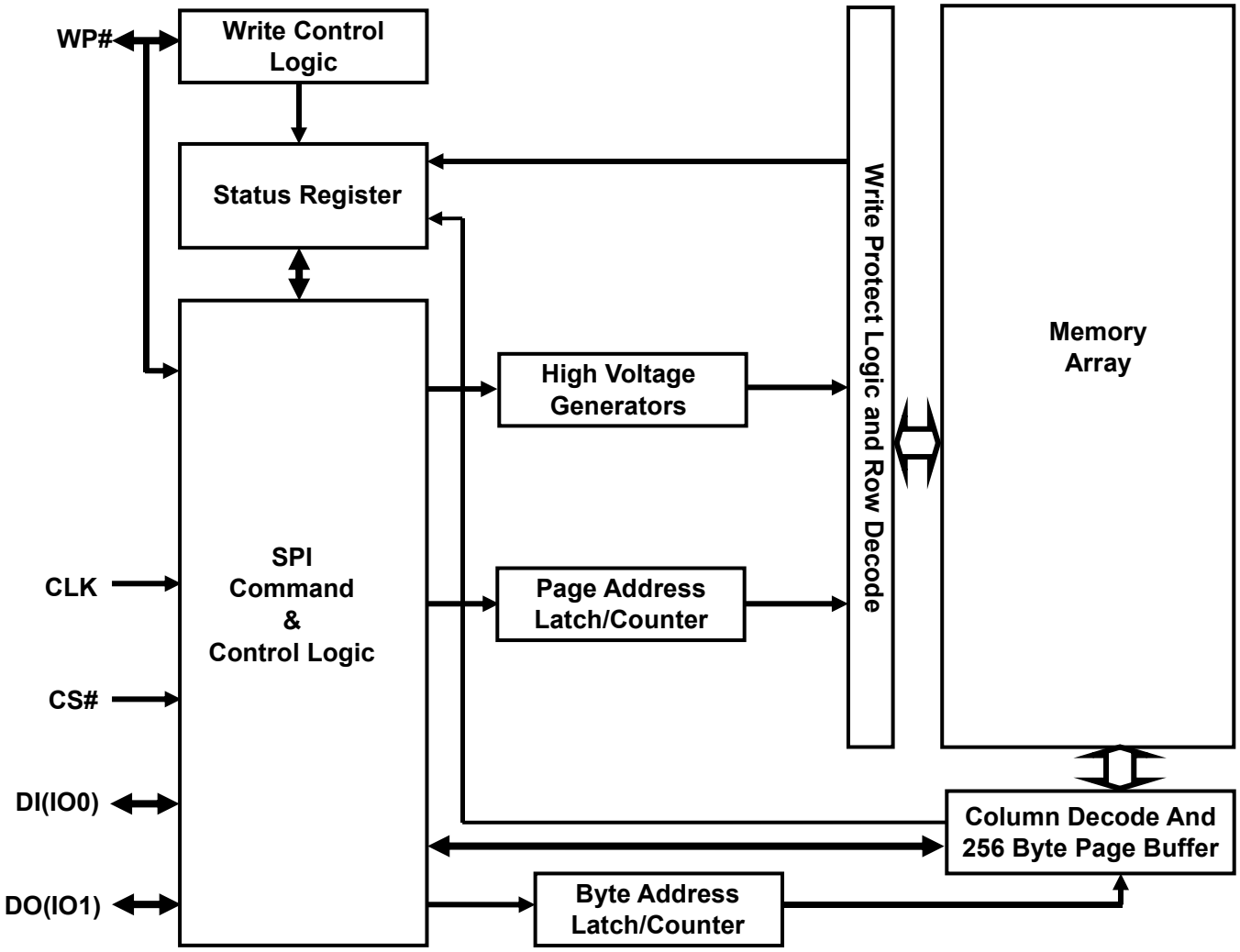
## 3.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions

## 4. BLOCK DIAGRAM



## 5.Memory Architecture Diagram（2Mb）

| 64KB Block | 32KB Block | 4KB Block | Block Address Range | 256Byte Page | Page Address Range |
|---|---|---|---|---|---|
| 64KB | 32KB | 4KB | 03FFFFh – 03F000h | 256 Bytes | 03FFFFh – 03FF00h |
| | | 4KB | 03EFFFh – 03E000h | 256 Bytes | 03FEFFh – 03FE00h |
| | | 4KB | 03DFFFh – 03D000h | 256 Bytes | 03FDFFh – 03FD00h |
| | | 4KB | 03CFFFh – 03C000h | 256 Bytes | 03FCFFh – 03FC00h |
| | | 4KB | 03BFFFh – 03B000h | 256 Bytes | 03FBFFh – 03FB00h |
| | | 4KB | 03AFFFh – 03A000h | 256 Bytes | 03FAFFh – 03FA00h |
| | | 4KB | 039FFFh – 039000h | 256 Bytes | 03F9FFh – 03F900h |
| | | 4KB | 038FFFh – 038000h | 256 Bytes | 03F8FFh – 03F800h |
| | 32KB | 4KB | 037FFFh – 037000h | 256 Bytes | 03F7FFh – 03F700h |
| | | 4KB | 036FFFh – 036000h | 256 Bytes | 03F6FFh – 03F600h |
| | | 4KB | 035FFFh – 035000h | 256 Bytes | 03F5FFh – 03F500h |
| | | 4KB | 034FFFh – 034000h | 256 Bytes | 03F4FFh – 03F400h |
| | | 4KB | 033FFFh – 033000h | 256 Bytes | 03F3FFh – 03F300h |
| | | 4KB | 032FFFh – 032000h | 256 Bytes | 03F2FFh – 03F200h |
| | | 4KB | 031FFFh – 031000h | 256 Bytes | 03F1FFh – 03F100h |
| | | 4KB | 030FFFh – 030000h | 256 Bytes | 03F0FFh – 03F000h |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| 64KB | 32KB | 4KB | 00FFFFh – 00F000h | 256 Bytes | 000FFFh – 000F00h |
| | | 4KB | 00EFFFh – 00E000h | 256 Bytes | 000EFFh – 000E00h |
| | | 4KB | 00DFFFh – 00D000h | 256 Bytes | 000DFFh – 000D00h |
| | | 4KB | 00CFFFh – 00C000h | 256 Bytes | 000CFFh – 000C00h |
| | | 4KB | 00BFFFh – 00B000h | 256 Bytes | 000BFFh – 000B00h |
| | | 4KB | 00AFFFh – 00A000h | 256 Bytes | 000AFFh – 000A00h |
| | | 4KB | 009FFFh – 009000h | 256 Bytes | 0009FFh – 000900h |
| | | 4KB | 008FFFh – 008000h | 256 Bytes | 0008FFh – 000800h |
| | 32KB | 4KB | 007FFFh – 007000h | 256 Bytes | 0007FFh – 000700h |
| | | 4KB | 006FFFh – 006000h | 256 Bytes | 0006FFh – 000600h |
| | | 4KB | 005FFFh – 005000h | 256 Bytes | 0005FFh – 000500h |
| | | 4KB | 004FFFh – 004000h | 256 Bytes | 0004FFh – 000400h |
| | | 4KB | 003FFFh – 003000h | 256 Bytes | 0003FFh – 000300h |
| | | 4KB | 002FFFh – 002000h | 256 Bytes | 0002FFh – 000200h |
| | | 4KB | 001FFFh – 001000h | 256 Bytes | 0001FFh – 000100h |
| | | 4KB | 000FFFh – 000000h | 256 Bytes | 0000FFh – 000000h |

# 6. ELECTRICAL CHARACTERISTICS

## 6.1 Absolute Maximum Ratings(1)

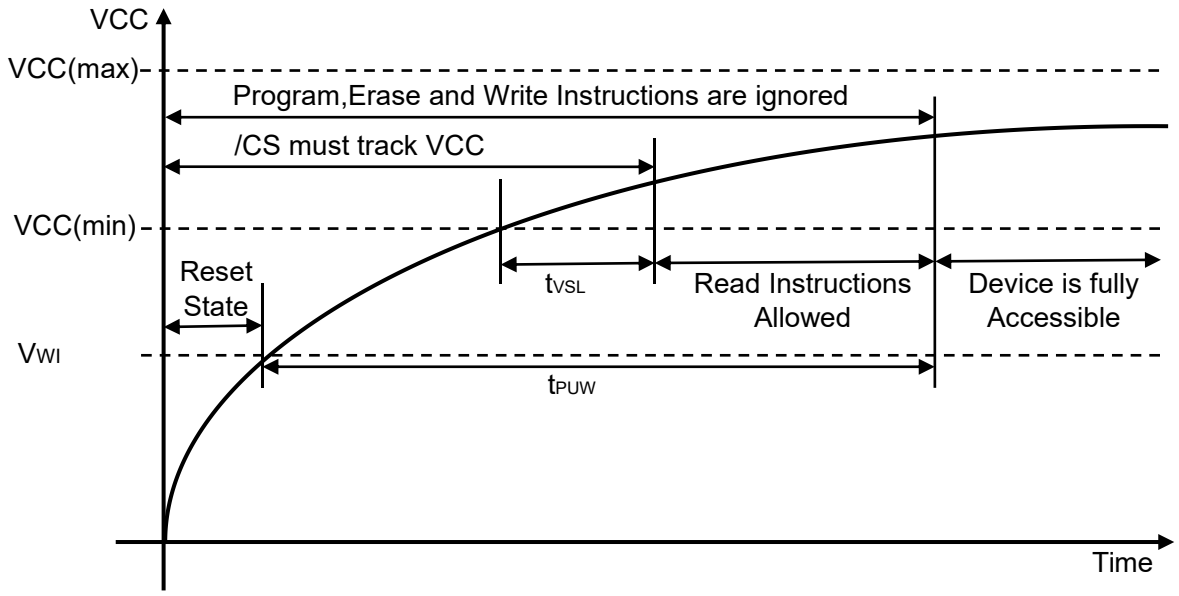
| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | -0.6 to VCC+0.6V | V |
| Voltage Applied to Any Pin | V IO | Relative to Ground | -0.6 to VCC+0.4V | V |
| Transient Voltage on any Pin | VIOT | <20nS Transient Relative to Ground | -2.0V to VCC+2.0V | V |
| Storage Temperature | TSTG | | –65 to +150 °C | °C |
| Ambient Operating Temperature | Ta | | –40 to +85/105 °C | °C |
| Electrostatic Discharge Voltage | VESD | Human Body Model(2) | –4000 to +4000 V | V |

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

2. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

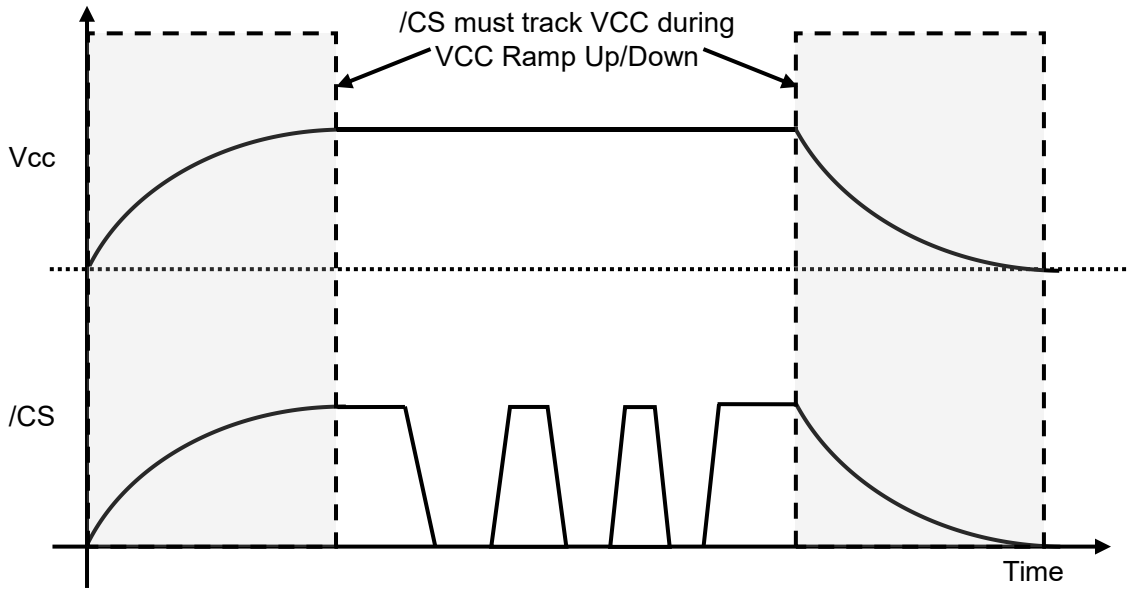
## 6.2 Power-up Timing and Write Inhibit Threshold

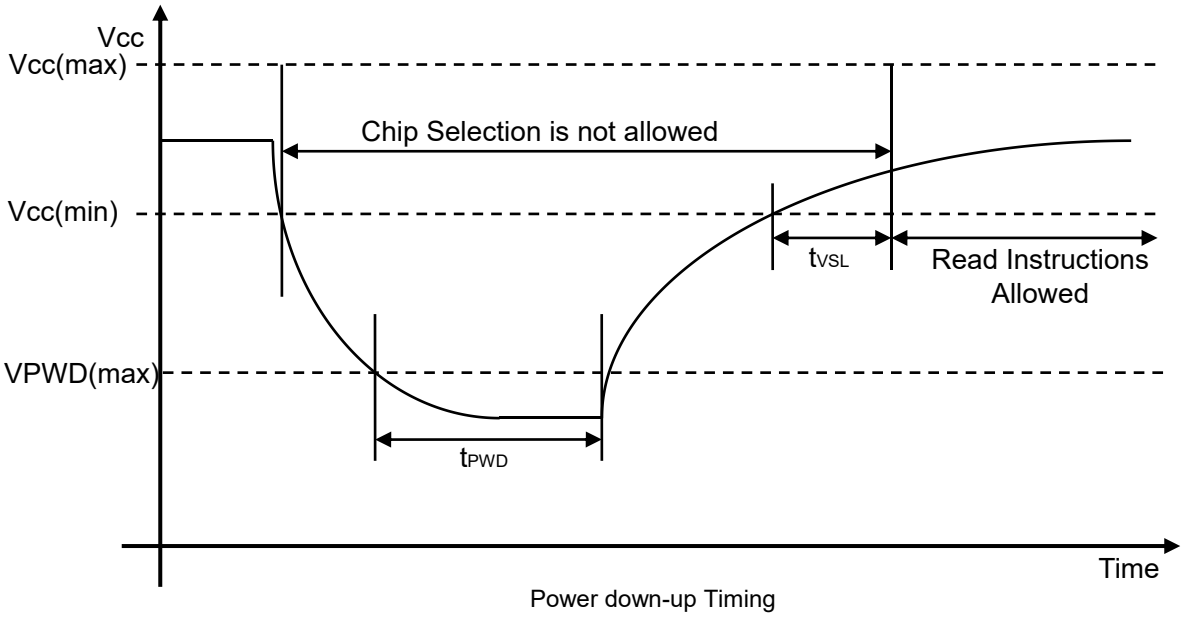



Power-up Timing and Voltage Levels

| PARAMETERS | SYMBOL | spec | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| VCC (min) to /CS Low | tVSL(1) | 100 | | µs |
| Time Delay Before Write Instruction | tPUW(1) | 5 | | ms |
| Write Inhibit Threshold Voltage | VWI(1) | 1.2 | 1.4 | V |

## 6.3 Power Up/Down and Voltage Drop




Power down-up Timing

| Symbol | Parameter | min | max | unit |
|---|---|---|---|---|
| $V_{PWD}$ | VCC voltage needed to below VPWD for ensuring initialization will occur | | 0.5 | V |
| $t_{PWD}$ | The minimum duration for ensuring initialization will occur | 300 | | us |
| $t_{VR}$ | VCC Rise Time | 1 | 500000 | us/V |

## 6.4 DC Electrical Characteristics:

（Ta= -40℃~85℃，VCC=1.65~3.6V）

| Symbol | Paraneter | Conditions | 1.65 to 2.3V | | | 2.3to 3.6V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | *Min.* | *Typ.* | *Max.* | |
| ISB | Standby Current | CS#=Vcc, all other inputs at 0V or Vcc | | 7.0 | 35 | | 7.0 | 35 | μA |
| IDBD | Deep power down current | CS#=Vcc, all other inputs at 0V or Vcc | | 0.05 | 3.0 | | 0.1 | 5.0 | μA |
| ICC1 | Current Read Data | Fr=33MHz DO=Open | | 0.8 | 4.0 | | 1.8 | 4.0 | mA |
| | | Fr=50MHz DO=Open | | 1.0 | 6.0 | | 2.0 | 6.0 | mA |
| | | Fr=104MHz DO=Open | | 1.8 | 8.0 | | 3.5 | 8.0 | mA |
| ICC3 | Program current | CS#=Vcc | | 0.5 | 2.0 | | 1.3 | 3.0 | mA |
| ICC4 | Erase Current 4K,1K | CS#=Vcc | | 0.7 | 2.0 | | 1.0 | 4.0 | mA |
| ICC5 | Erase Current 32K | CS#=Vcc | | 0.7 | 2.5 | | 1.5 | 6.0 | mA |
| ICC6 | Erase Current 64K | CS#=Vcc | | 0.7 | 3.0 | | 1.5 | 8.0 | mA |
| ICC7 | Erase Current Chip | CS#=Vcc | | 0.7 | 4.0 | | 2.0 | 10 | mA |
| ILI | Input Leakage Current | | | 0.2 | 0.5 | | 0.5 | 1 | μA |
| ILO | Output Leakage Current | | | 0.2 | 0.5 | | 0.5 | 1 | μA |
| VIL | Input Low Voltage | | -0.5 | | 0.3VCC | -0.5 | | 0.3VCC | V |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | 0.7VCC | | VCC+0.4 | V |
| VOL | Output Low Voltage | IOL=100μA | | | 0.2 | | | 0.2 | V |
| VOH | Output High Voltage | IOH=-100μA | VCC-0.2 | | | VCC-0.2 | | | V |

**Note:**

1. Typical values measured at 3.0V @ 25°C for the 1.65V to 3.6V range.

## 6.5 DC Electrical Characteristics:

（Ta= -40℃~105℃，VCC=1.65~3.6V）

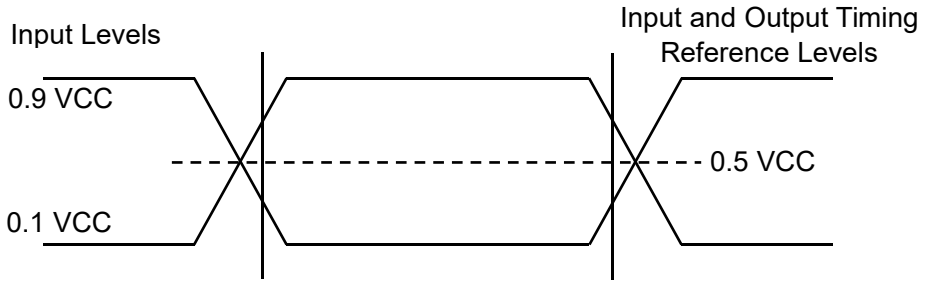
| Symbol | Paraneter | Conditions | 1.65 to 2.3V | | | 2.3to 3.6V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | *Min.* | *Typ.* | *Max.* | |
| ISB | Standby Current | CS#=Vcc, all other inputs at 0V or Vcc | | 7.0 | 50 | | 7.0 | 60 | μA |
| IDBD | Deep power down current | CS#=Vcc, all other inputs at 0V or Vcc | | 0.05 | 5.0 | | 0.1 | 8.0 | μA |
| ICC1 | Current Read Data | Fr=33MHz DO=Open | | 0.8 | 6.0 | | 1.8 | 6.0 | mA |
| | | Fr=50MHz DO=Open | | 1.0 | 8.0 | | 2.0 | 8.0 | mA |
| | | Fr=104MHz DO=Open | | 1.8 | 10 | | 3.5 | 10 | mA |
| ICC3 | Program current | CS#=Vcc | | 0.5 | 4.0 | | 1.3 | 5.0 | mA |
| ICC4 | Erase Current 4K,1K | CS#=Vcc | | 0.7 | 4.0 | | 1.0 | 6.0 | mA |
| ICC5 | Erase Current 32K | CS#=Vcc | | 0.7 | 5.0 | | 1.5 | 8.0 | mA |
| ICC6 | Erase Current 64K | CS#=Vcc | | 0.7 | 6.0 | | 1.5 | 10 | mA |
| ICC7 | Erase Current Chip | CS#=Vcc | | 0.7 | 8.0 | | 2.0 | 12 | mA |
| ILI | Input Leakage Current | | | 0.2 | 0.5 | | 0.5 | 1 | μA |
| ILO | Output Leakage Current | | | 0.2 | 0.5 | | 0.5 | 1 | μA |
| VIL | Input Low Voltage | | -0.5 | | 0.3VCC | -0.5 | | 0.3VCC | V |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | 0.7VCC | | VCC+0.4 | V |
| VOL | Output Low Voltage | IOL=100μA | | | 0.2 | | | 0.2 | V |
| VOH | Output High Voltage | IOH=-100μA | VCC-0.2 | | | VCC-0.2 | | | V |

**Note:**

1. Typical values measured at 3.0V @ 25°C for the 1.65V to 3.6V range.

## 6.6 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Load Capacitance | CL | | 30 | Pf |
| Input Rise and Fall Times | TR,TF | | 5 | ns |
| Input Pulse Voltages | VIN | 0.1 VCC to 0.9 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to 0.7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC to 0.5 VCC | | V |




AC Measurement I/O Waveform

## 6.7 AC Characteristics

（Ta= -40℃~85℃，VCC=1.65~3.6V）

| Symbol | Description | 1.65V~3.6V | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Fr/Fc | Clock frequency for all instructions vdd from 1.65-2.3V except Read Data (03h) | D.C. | | 50 | MHz |
| | Clock frequency for all instructions vdd from 2.3-2.7V except Read Data (03h) | D.C. | | 90 | MHz |
| | Clock frequency for all instructions vdd from 2.7-3.6V except Read Data (03h)(5) | D.C. | | 104 | MHz |
| | Clock frequency for all instructions vdd from1.65-2.7V for Read Data (03h) | D.C. | | 30 | MHz |
| | Clock frequency for all instructions vdd from 2.7-3.6V for Read Data (03h) | D.C. | | 40 | MHz |
| Tch(1) | Clock High Time | 45% (1/Fc) | | | ns |
| Tcl(1) | Clock Low Time | 45% (1/Fc) | | | ns |
| Tclch(4) | Clock Rise Time peak to peak | 0.1 | | | V/ns |
| Tchcl(4) | Clock Fall Time peak to peak | 0.1 | | | V/ns |
| Tslch | CS# Active Setup Time (relative to CLK, Vcc=2.3v~3.6v) | 7 | | | ns |
| Tslch | CS# Active Setup Time (relative to CLK, Vcc=1.65v~2.3v) | 10 | | | ns |
| Tchsl | CS# Not Active Hold Time (relative to CLK) | 5 | | | ns |
| Tdvch | Data In Setup Time | 2 | | | ns |
| Tchdx | Data In Hold Time | 5 | | | ns |
| Tchsh | CS# Active Hold Time (relative to CLK) | 5 | | | ns |

| Symbol | Description | 1.65V~3.6V | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Tshch | CS# Not Active Setup Time (relative to CLK) | 10 | | | ns |
| Tshsl | CS# Deselect Time From Read to next Read | 15 | | | ns |
| | CS# Deselect Time From Erase,Program to Read Status Register | 30 | | | ns |
| Tshqz(4) | Output Disable Time | | | 11 | ns |
| Tclqv(6) | Clock Low to Output Valid (Vcc=2.3v~3.6v) | | 5 | 12 | ns |
| | Clock Low to Output Valid (Vcc=1.65v~2.3v) | | 7 | 15 | ns |
| Tclqx | Output Hold Time | 0 | | | ns |
| Twhsl(3) | Write Protect Setup Time | 20 | | | ns |
| Tshwl(3) | Write Protect Hold Time | 100 | | | ns |
| Tdp | CS# High to Deep Power-down Mode | | | 3 | us |
| Tres1 | CS# High To Standby Mode Without ID Read | | 5 | 20 | us |
| Tres2 | CS# High To Standby Mode With ID Read | | 5 | 20 | us |
| Trst | CS# High to next Instruction after reset （except chip erase 60/C7h） | | | 30 | μs |
| | CS# High to Chip erase after reset | | 100 | 150 | us |
| Tw | Write Status Register Cycle Time | | 2.5 | 4.0 | ms |
| Tbp | Byte Program Time (First Byte) | | 80 | 150 | μs |
| Tpp | Page Program Time | | 1.3 | 2.5 | ms |
| Tse | Sector erase time | | 2.5 | 7 | ms |
| Tbe1 | Block erase time for 32K bytes | | 2.5 | 7 | ms |
| Tbe2 | Block erase time for 64K bytes | | 2.5 | 7 | ms |
| Tce | Chip erase time | | 5 | 13 | ms |

**Note:**

1. Tch + Tcl must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. The value guaranteed by characterization, not 100% tested in production.
5. If in high speed application, suggest to configure the drive strength to 100% which will appropriately increase the value of Tclqv and clock frequency to meet the application requirement.
6. The Tclqv parameter are tested on sample basis and specified through design and characterization data, TA = 25° C. The typical value are measured at DRV≥25% condition, and the max value are measured at DRV=10%.

## 6.8 AC Characteristics

（Ta= -40℃~105℃，VCC=1.65~3.6V）

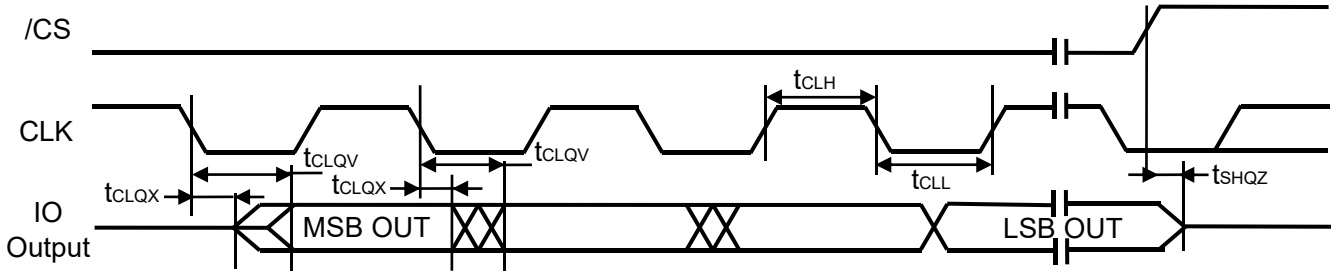
| Symbol | Description | 1.65V~3.6V | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Fr/Fc | Clock frequency for all instructions vdd from 1.65-2.7V except Read Data (03h) | D.C. | | 50 | MHz |
| | Clock frequency for all instructions vdd from 2.7-3.6V except Read Data (03h) | D.C. | | 90 | MHz |
| | Clock frequency for all instructions vdd from 2.7-3.6V except Read Data (03h)(5) | D.C. | | 104 | MHz |
| | Clock frequency for all instructions vdd from1.65-2.7V for Read Data (03h) | D.C. | | 30 | MHz |
| | Clock frequency for all instructions vdd from 2.7-3.6V for Read Data (03h) | D.C. | | 40 | MHz |
| Tch(1) | Clock High Time | 45% (1/Fc) | | | ns |
| Tcl(1) | Clock Low Time | 45% (1/Fc) | | | ns |
| Tclch(4) | Clock Rise Time peak to peak | 0.1 | | | V/ns |
| Tchcl(4) | Clock Fall Time peak to peak | 0.1 | | | V/ns |
| Tslch | CS# Active Setup Time (relative to CLK, Vcc=2.3v~3.6v) | 7 | | | ns |
| Tslch | CS# Active Setup Time (relative to CLK, Vcc=1.65v~2.3v) | 10 | | | ns |
| Tchsl | CS# Not Active Hold Time (relative to CLK) | 5 | | | ns |
| Tdvch | Data In Setup Time | 2 | | | ns |
| Tchdx | Data In Hold Time | 5 | | | ns |
| Tchsh | CS# Active Hold Time (relative to CLK) | 5 | | | ns |
| Tshch | CS# Not Active Setup Time (relative to CLK) | 10 | | | ns |
| Tshsl | CS# Deselect Time From Read to next Read | 15 | | | ns |
| | CS# Deselect Time From Erase,Program to Read Status Register | 30 | | | ns |
| Tshqz(4) | Output Disable Time | | | 11 | ns |
| Tclqv(6) | Clock Low to Output Valid (Vcc=2.3v~3.6v) | | 5 | 12 | ns |
| | Clock Low to Output Valid (Vcc=1.65v~2.3v) | | 7 | 15 | ns |
| Tclqx | Output Hold Time | 0 | | | ns |
| Twhsl(3) | Write Protect Setup Time | 20 | | | ns |
| Tshwl(3) | Write Protect Hold Time | 100 | | | ns |
| Tdp | CS# High to Deep Power-down Mode | | | 3 | us |
| Tres1 | CS# High To Standby Mode Without ID Read | | 5 | 20 | us |
| Tres2 | CS# High To Standby Mode With ID Read | | 5 | 20 | us |
| Trst | CS# High to next Instruction after reset（except chip erase 60/C7h） | | | 30 | μs |
| | CS# High to Chip erase after reset | | 100 | 150 | us |
| Tw | Write Status Register Cycle Time | | 2.5 | 4.0 | ms |
| Tbp | Byte Program Time (First Byte) | | 80 | 150 | μs |

| Symbol | Description | 1.65V~3.6V | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Tpp | Page Program Time | | 1.3 | 2.5 | ms |
| Tse | Sector erase time | | 2.5 | 7 | ms |
| Tbe1 | Block erase time for 32K bytes | | 2.5 | 7 | ms |
| Tbe2 | Block erase time for 64K bytes | | 2.5 | 7 | ms |
| Tce | Chip erase time | | 5 | 13 | ms |

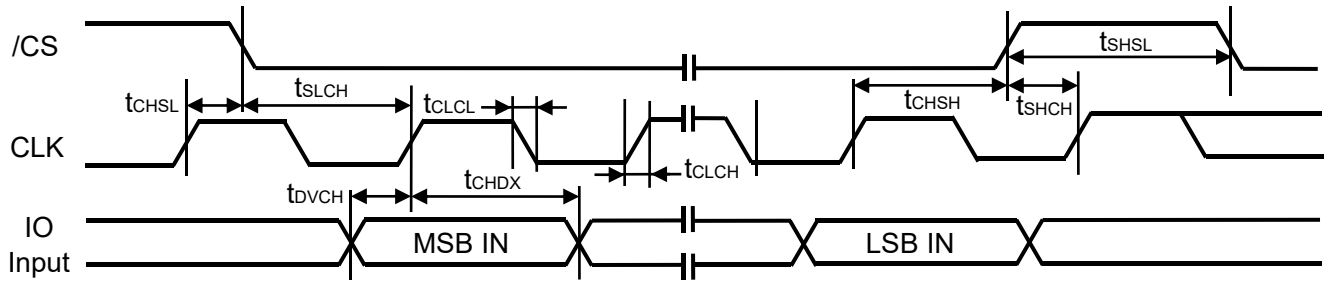
**Note:**

1. Tch + Tcl must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. The value guaranteed by characterization, not 100% tested in production.
5. If in high speed application, suggest to configure the drive strength to 100% which will appropriately increase the value of Tclqv and clock frequency to meet the application requirement.
6. The Tclqv parameter are tested on sample basis and specified through design and characterization data, TA = 25° C. The typical value are measured at DRV≥25% condition, and the max value are measured at DRV=10%.

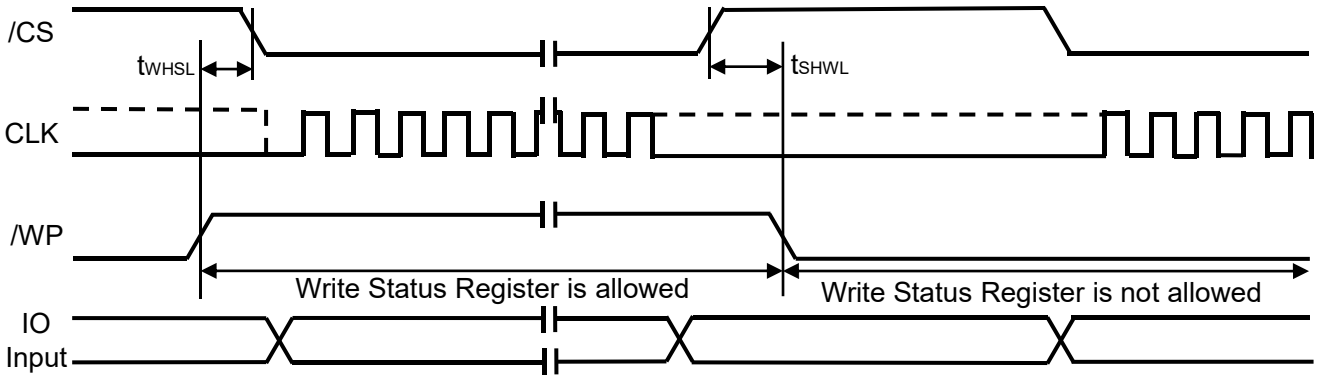
## 6.9 Serial Output Timing




## 6.10 Serial Input Timing




## 6.11 /WP Timing



# 7 FUNCTIONAL DESCRIPTION

## 7.1 Standard SPI Instructions

The GT25D20/10/05E is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

## 7.2 Dual SPI Instructions

The GT25D20/10/05E supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

## 7.5 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the GT25D20/10/05E provides several means to protect the data from inadvertent writes.

## 7.6 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up

Upon power-up or at power-down, the GT25D20/10/05E will maintain a reset condition while VCC is below the threshold value of VWI, (See Power-up Timing and Voltage Levels). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of Tpuw. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and Tvsl time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

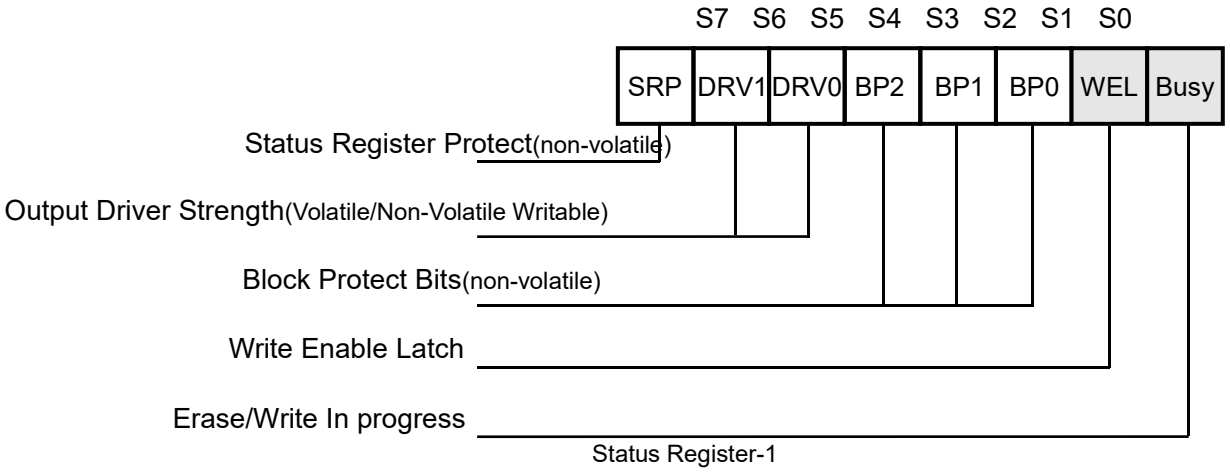
Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (BP2, BP1 and BP0) bits. These settings allow a portion as small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status

Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

# 8 STATUS REGISTERS AND INSTRUCTIONS

The Read Status Register-1 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection. The Write Status Register instruction can be used to configure the device write protection features. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

## 8.1 STATUS REGISTER 1




Status Register-1

### 8.1.1 BUSY Status (BUSY)

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see Tw, Tpp, Tse, Tbe, and Tce in AC Characteristics),and each Read Status Register must pull down and up CS#. When the program, erase instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

### 8.1.2 Write Enable Latch Status (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register.

### 8.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see Tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

### 8.1.4 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

| DRV1 | DRV0 | Driver Strength |
|---|---|---|
| 0 | 0 | 100% |
| 0 | 1 | 50% |
| 1 | 0 | 25% |
| 1 | 1 | 10% |

Note:
1. It is recommended to use 100% DVR for 1.8v application, 10% DVR for 3.3v application, and the Default value of S5 and S6 shall be subject to the goods actually received.

### 8.1.5 Status Register Protect (SRP)

The Status Register Protect (SRP) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

| SRP | /WP | Status Protection | Description |
|---|---|---|---|
| 0 | X | Software Protection | /WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default] |
| 1 | 0 | Hardware Protected | When /WP pin is low the Status Register can not be written to. |
| 1 | 1 | Hardware Unprotected | When /WP pin is high the Status register can be written to after a Write Enable instruction, WEL=1. |

## 8.2 Status Register Memory Protection

**Status Register Memory Protection Table1**

| GT25D20E (2M-BIT) MEMORY PROTECTION(2) | | | | | | |
|---|---|---|---|---|---|---|
| BP2 | BP1 | BP0 | BLOCK(S) | ADDRESSES | DENSITY | PORTION |
| 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 1 | 0 thru 3 | 000000h –03DFFFh | 248KB | Lower 31/32 |
| 0 | 1 | 0 | 0 thru 3 | 000000h –03BFFFh | 240KB | Lower 15/16 |
| 0 | 1 | 1 | 0 thru 3 | 000000h –037FFFh | 224KB | Lower7/8 |
| 1 | 0 | 0 | 0 thru 2 | 000000h –02FFFFh | 192KB | Lower 3/4 |
| 1 | 0 | 1 | 0 and1 | 000000h –01FFFFh | 128KB | Lower 1/2 |
| 1 | 1 | X | 0 thru 3 | 000000h –03FFFFh | 256KB | All |

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

## Status Register Memory Protection Table2

| GT25D10E (1M-BIT) MEMORY PROTECTION(2) | | | | | | |
|---|---|---|---|---|---|---|
| BP2 | BP1 | BP0 | BLOCK(S) | ADDRESSES | DENSITY | PORTION |
| 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 1 | 0 and1 | 000000h –01DFFFh | 120 KB | Lower 15/16 |
| 0 | 1 | 0 | 0 and1 | 000000h –01BFFFh | 112KB | Lower 7/8 |
| 0 | 1 | 1 | 0 and1 | 000000h –017FFFh | 96KB | Lower3/4 |
| 1 | 0 | 0 | 0 and1 | 000000h –00FFFFh | 64KB | Lower 1/2 |
| 1 | 0 | 1 | 0 and1 | 000000h –01FFFFh | 128KB | All |
| 1 | 1 | X | 0 and1 | 000000h –01FFFFh | 128KB | All |

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

## Status Register Memory Protection Table3

| GT25D05E (512K-BIT) MEMORY PROTECTION(2) | | | | | | |
|---|---|---|---|---|---|---|
| BP2 | BP1 | BP0 | BLOCK(S) | ADDRESSES | DENSITY | PORTION |
| 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 1 | 0 and1 | 000000h –00DFFFh | 56KB | Lower 7/8 |
| 0 | 1 | 0 | 0 and1 | 000000h –00BFFFh | 48KB | Lower3/4 |
| 0 | 1 | 1 | 0 and1 | 000000h –007FFFh | 32KB | Lower 1/2 |
| 1 | X | X | 0 and1 | 000000h –00FFFFh | 64KB | All |

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

# 9 Commands DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of CLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on DI, and each bit is latched on the rising edges of CLK.

See below Table, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

## 9.1 Commands Table

| Command Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte6 | Byte N |
|---|---|---|---|---|---|---|---|
| Write Enable | 06H | | | | | | |
| Write Disable | 04H | | | | | | |
| Read Status Register1 | 05H | S7-S0 | | | | | continuous |
| Write Status Register1 | 01H | S7-S0 | S15-S8 | | | | |
| Read Data | 03H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | Next byte | continuous |
| Fast Read | 0BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | continuous |
| Dual Output Fast Read | 3BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | continuous |
| Dual I/O Fast Read | BBH | A23-A8(2) | A7-A0 M7-M0(2) | (D7-D0)(1) | | | continuous |
| Page Program | 02H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | Next byte | |
| Sector Erase(4KB) | 20H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(32KB) | 52H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(64K) | D8H | A23-A16 | A15-A8 | A7-A0 | | | |
| Chip Erase | C7/60H | | | | | | |
| Enable Reset | 66H | | | | | | |
| Reset | 99H | | | | | | |
| Deep Power-Down | B9H | | | | | | |
| Release From Deep Power-Down, And Read Device ID | ABH | dummy | dummy | dummy | (ID7-ID0) | | continuous |
| Manufacturer / Device ID | 90H | dummy | dummy | 00h | (M7-M0) | (ID7-ID0) | continuous |
| Read Identification | 9FH | (M7-M0) | (ID15-ID8) | (ID7-ID0) | | | continuous |
| Read Unique ID | 4BH | dummy | dummy | dummy | dummy | UID63-0) | |

NOTE:
1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)

## 9.2 Manufacturer and Device Identification

| | Command | M7-M0 | ID15-ID8 | ID7-ID0 |
|---|---|---|---|---|
| GT25D20E | 9FH | C4h | 60 | 12 |
| | 90H | C4h | | 11 |
| | ABH | | | 11 |
| GT25D10E | 9FH | C4h | 60 | 11 |
| | 90H | C4h | | 10 |
| | ABH | | | 10 |
| GT25D05E | 9FH | C4h | 60 | 10 |
| | 90H | C4h | | 09 |
| | ABH | | | 09 |

## 9.3 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low →sending the Write Enable command → CS# goes high.

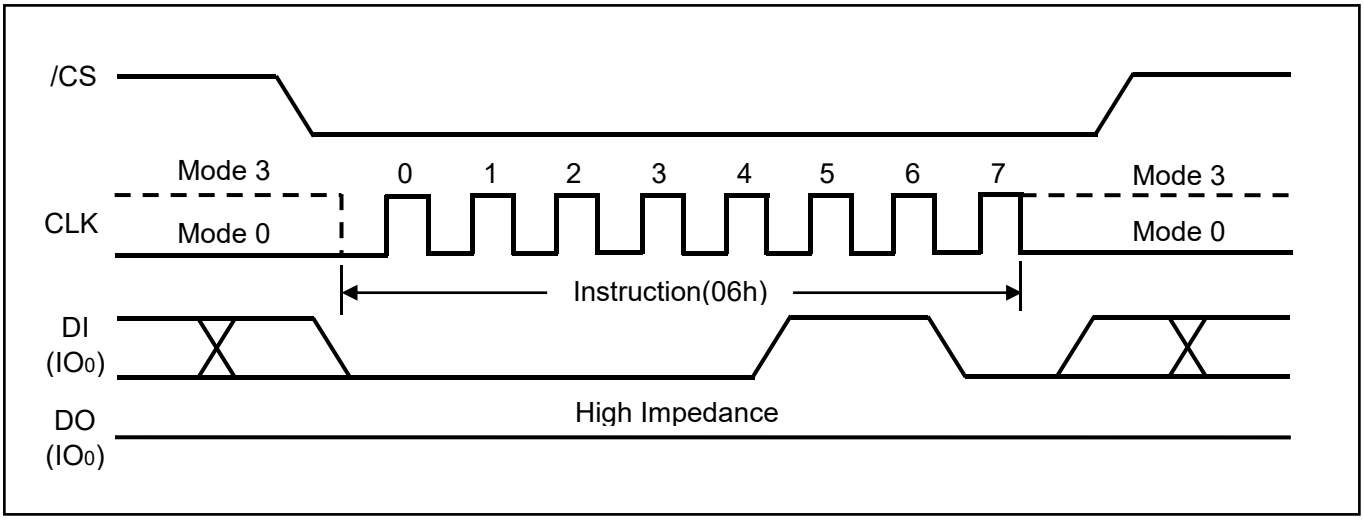



Figure1 Write Enable Sequence Diagram

## 9.4 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase and Reset commands.

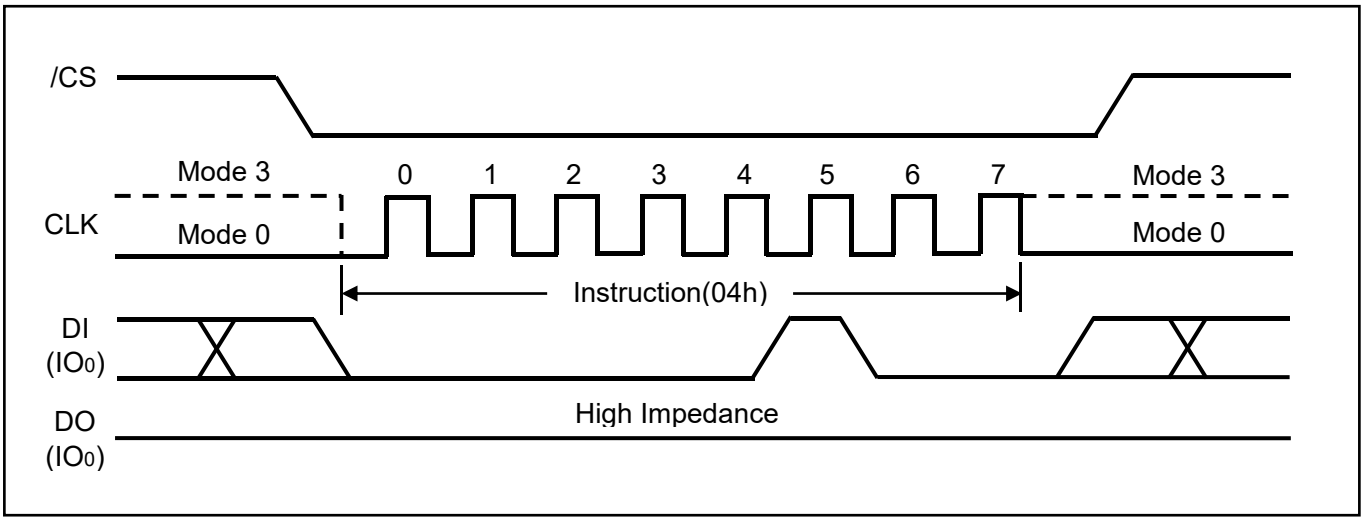



Figure2. Write Disable Sequence Diagram

## 9.5 Read Status Register (05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 4. The Status Register bits are shown in Status register1 include the BUSY, WEL, BP2-BP0,(see Status Register section earlier in this datasheet).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 3. The instruction is completed by driving /CS high.

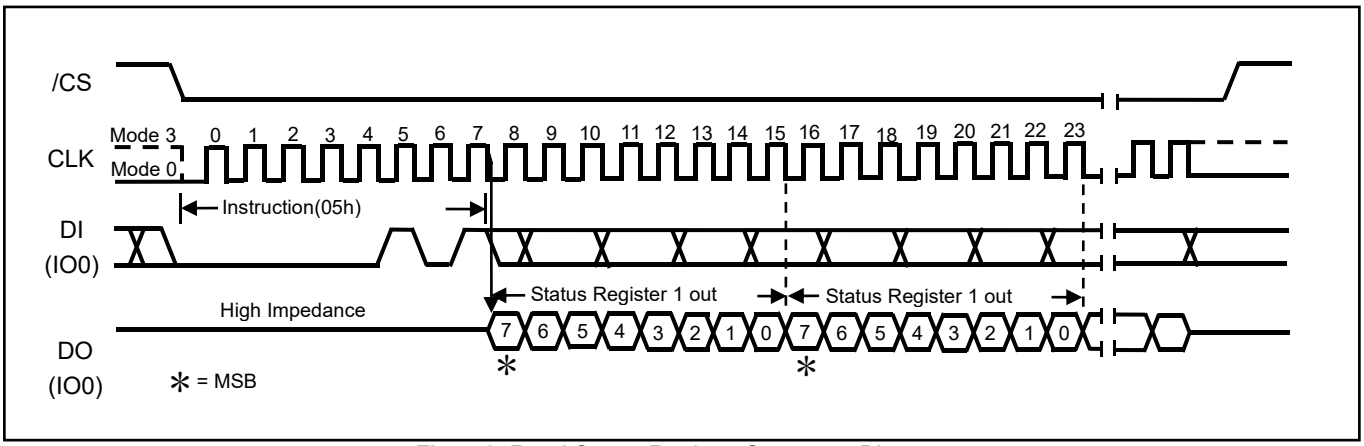



Figure3. Read Status Register Sequence Diagram

## 9.6 Write Status Register (WRSR) (01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, DR0,DR1, BP[2:0] in Status Register-1; All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 4.

During non-volatile Status Register write operation (06h combined with 01h, after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of Tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

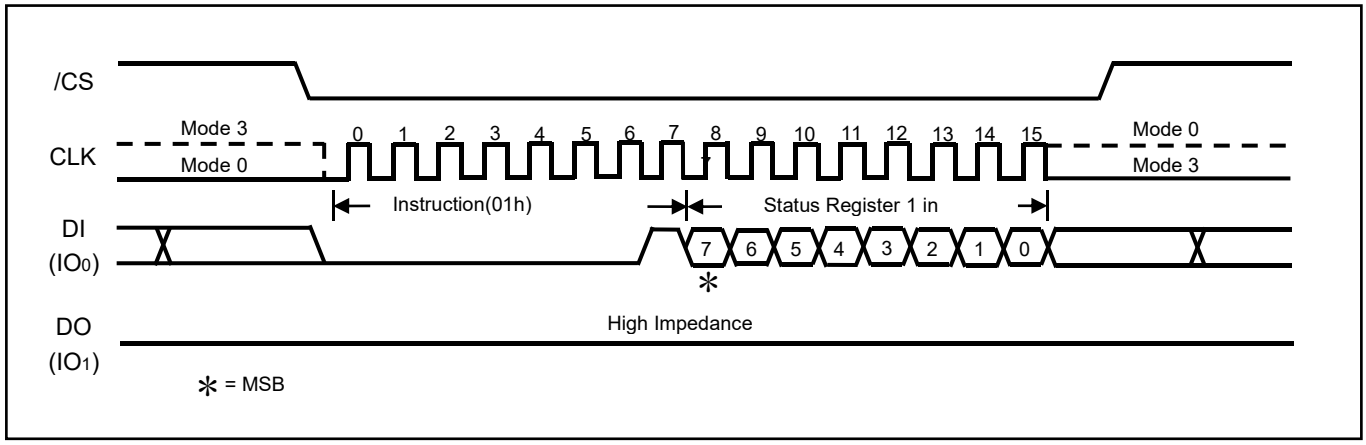



Figure4. Write Status Register Sequence Diagram

## 9.7 Read Data Bytes (READ) (03h)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), and each bit is latched-in on the rising edge of CLK. Then the memory content, at that address, is shifted out on DO, and each bit is shifted out, at a Max frequency Fr, on the falling edge of CLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

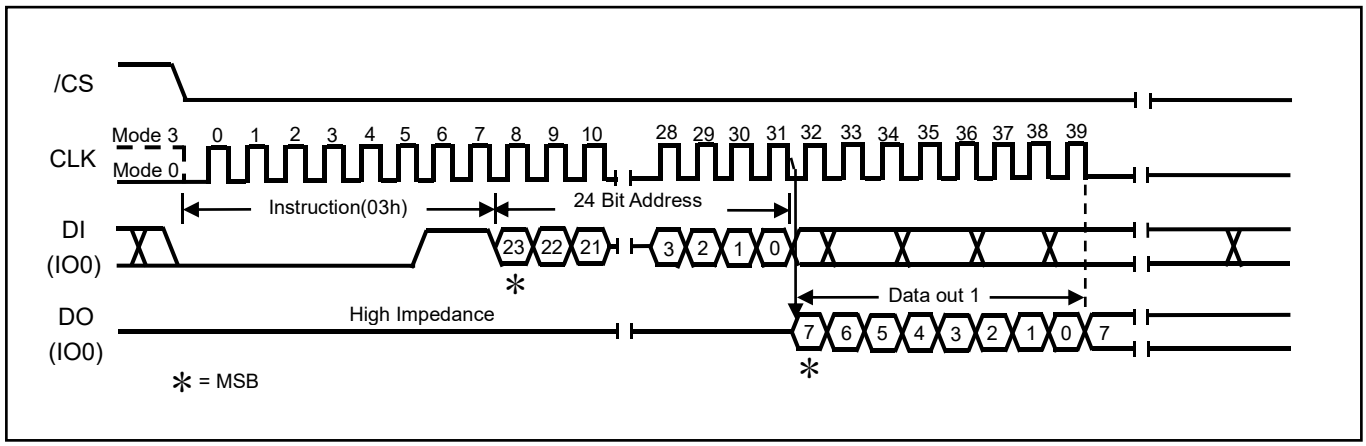



Figure5. Read Data Bytes Sequence Diagram

## 9.8 Fast Read (0Bh)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of CLK. Then the memory content, at that address, is shifted out on DO, and each bit is shifted out, at a Max frequency Fc, on the falling edge of CLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

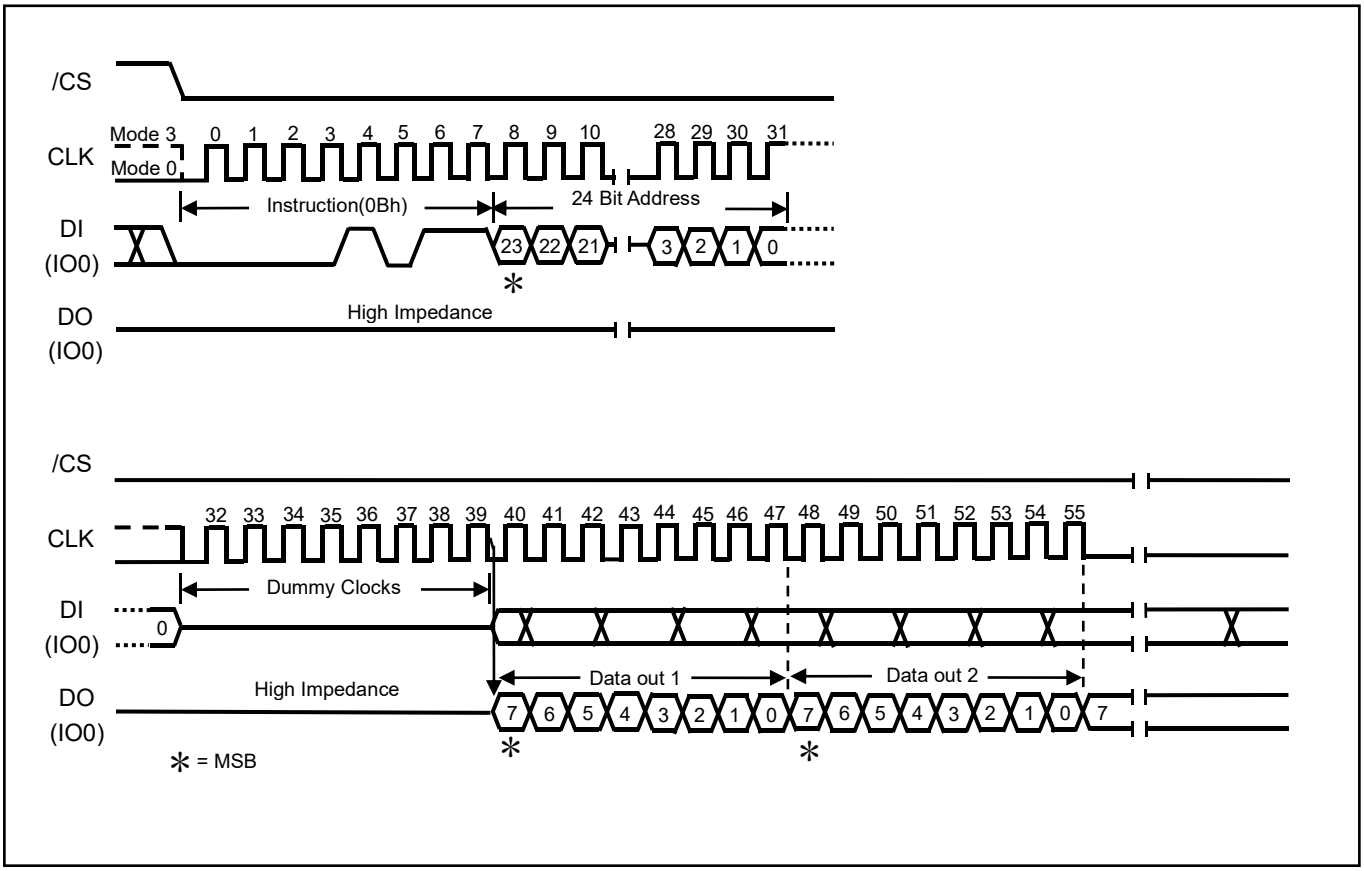



Figure6. Read Data Bytes at Higher Speed Sequence Diagram

## 9.9 Dual Output Fast Read (3Bh)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 2-bit per clock cycle from DI and DO.The command sequence is shown in followed Figure7. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

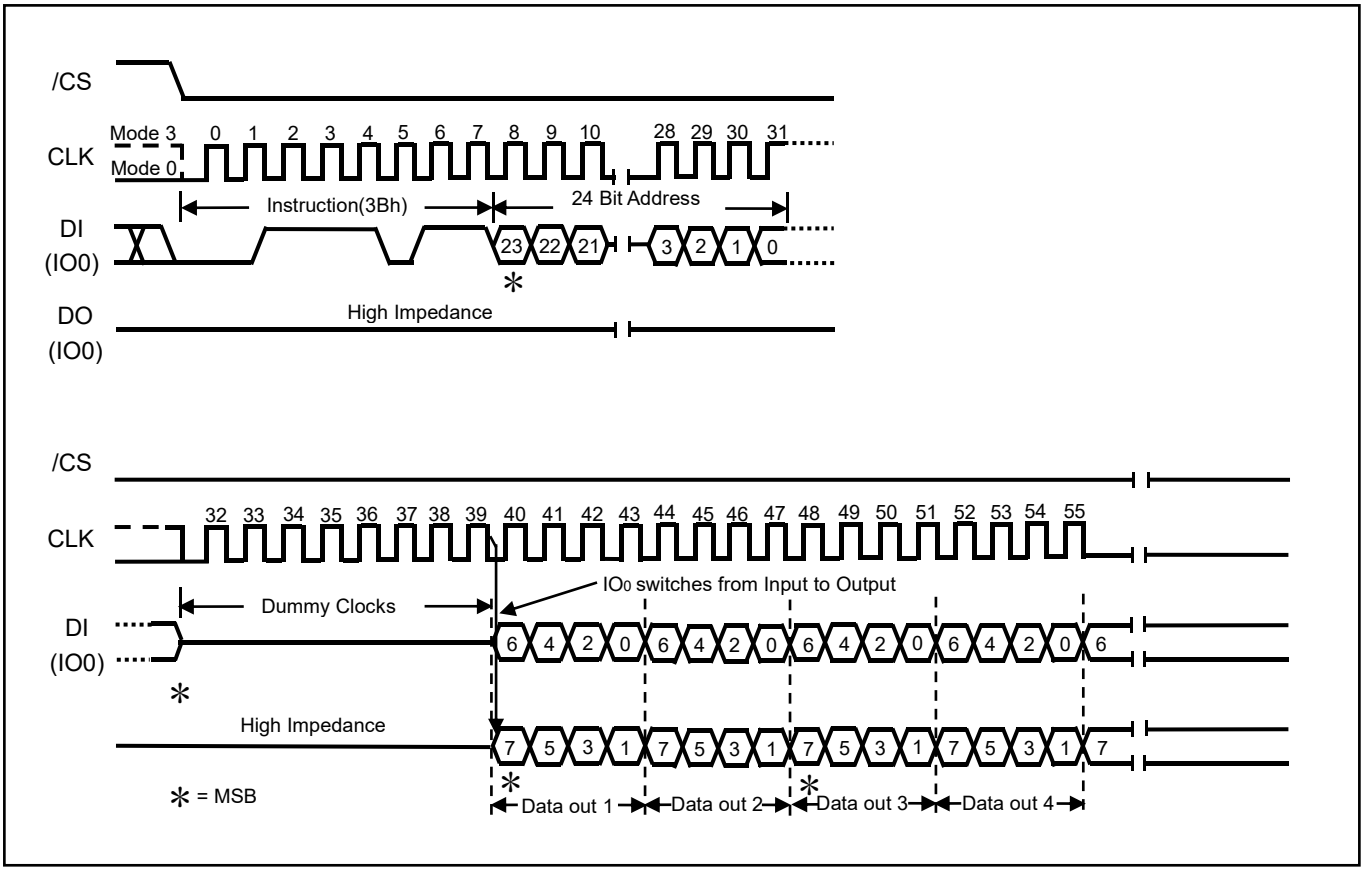



Figure7. Dual Output Fast Read Sequence Diagram

## 9.10 Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3- byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by DI and DO, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 2-bit per clock cycle from DI and DO. The command sequence is shown in followed Figure8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

**Dual I/O Fast Read with“Continuous Read Mode”**

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure8. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

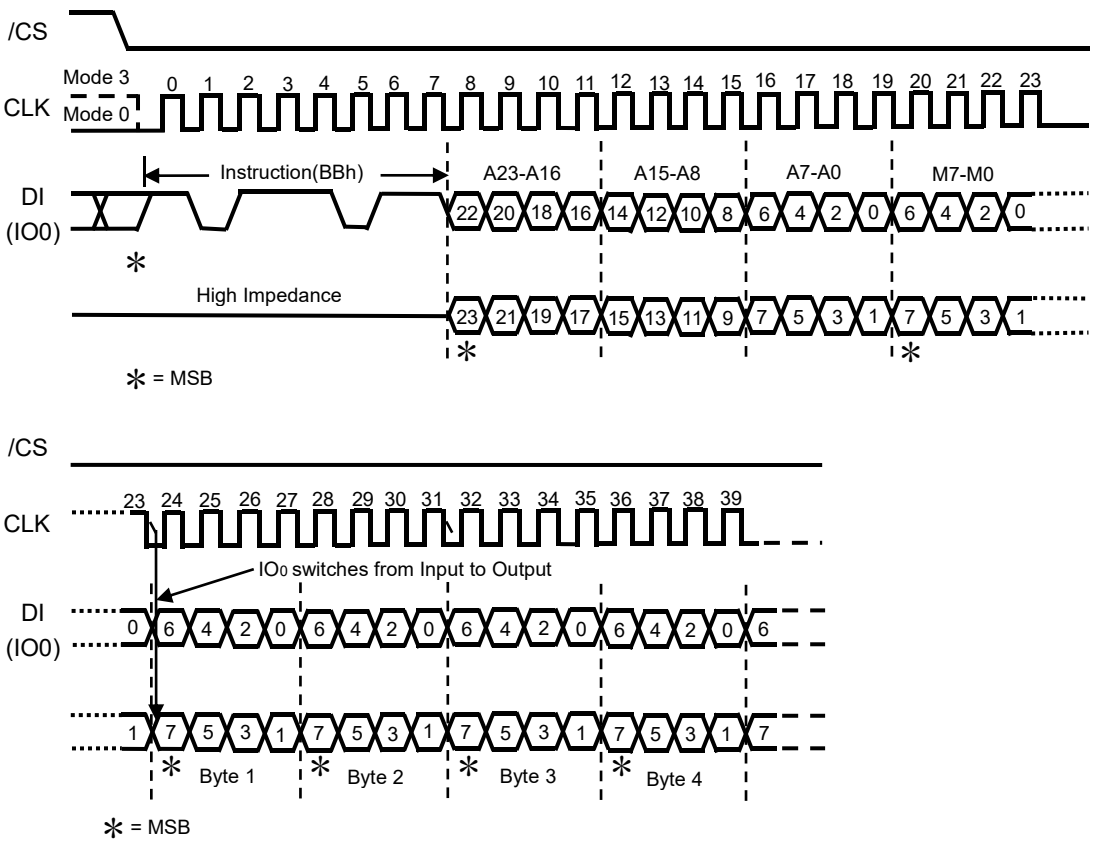



Figure8a. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

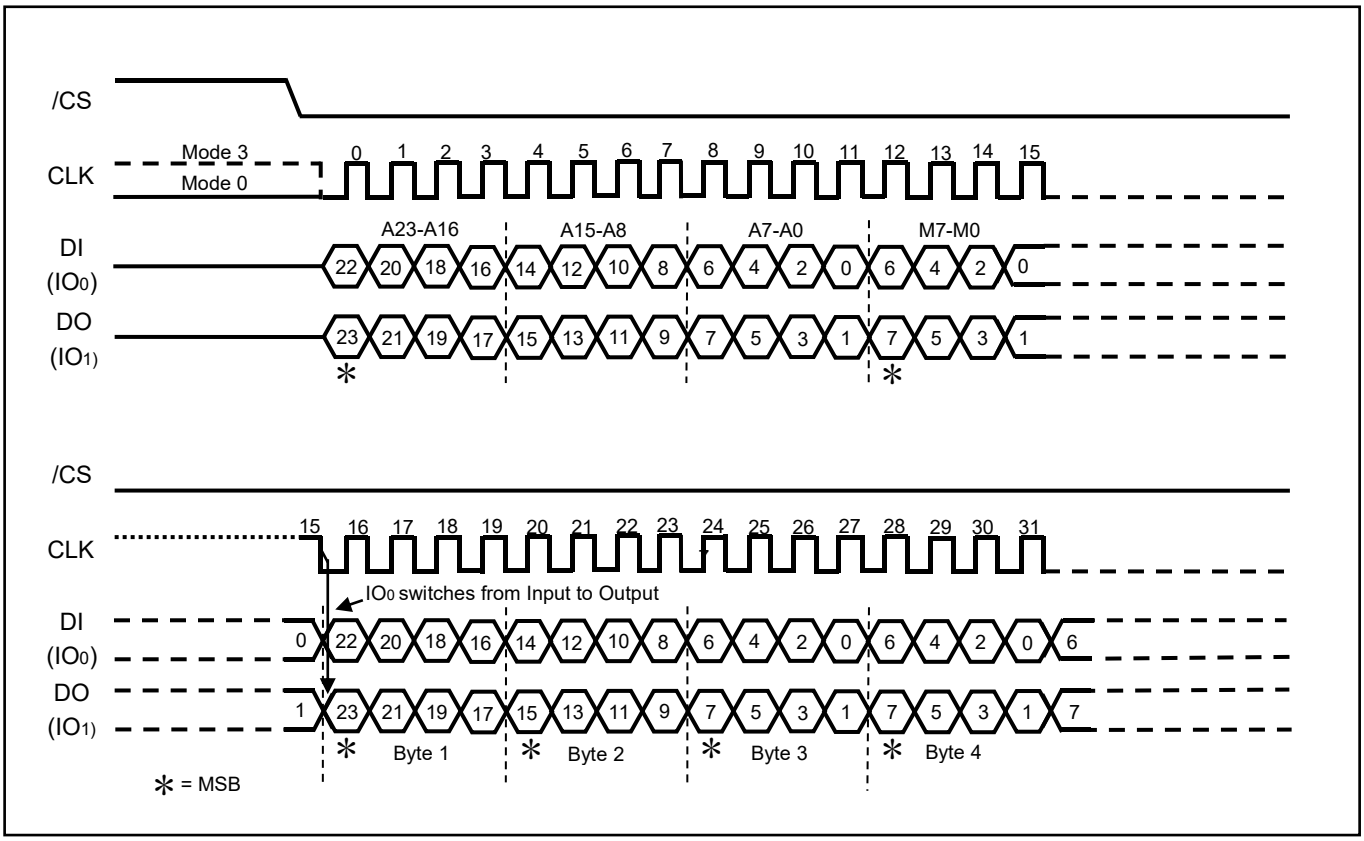



Figure8b. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))

## 9.11 Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on DI → at least 1 byte data on DI → CS# goes high. The command sequence is shown in Figure9. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is Tpp) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP2, BP1, and BP0) is not executed.

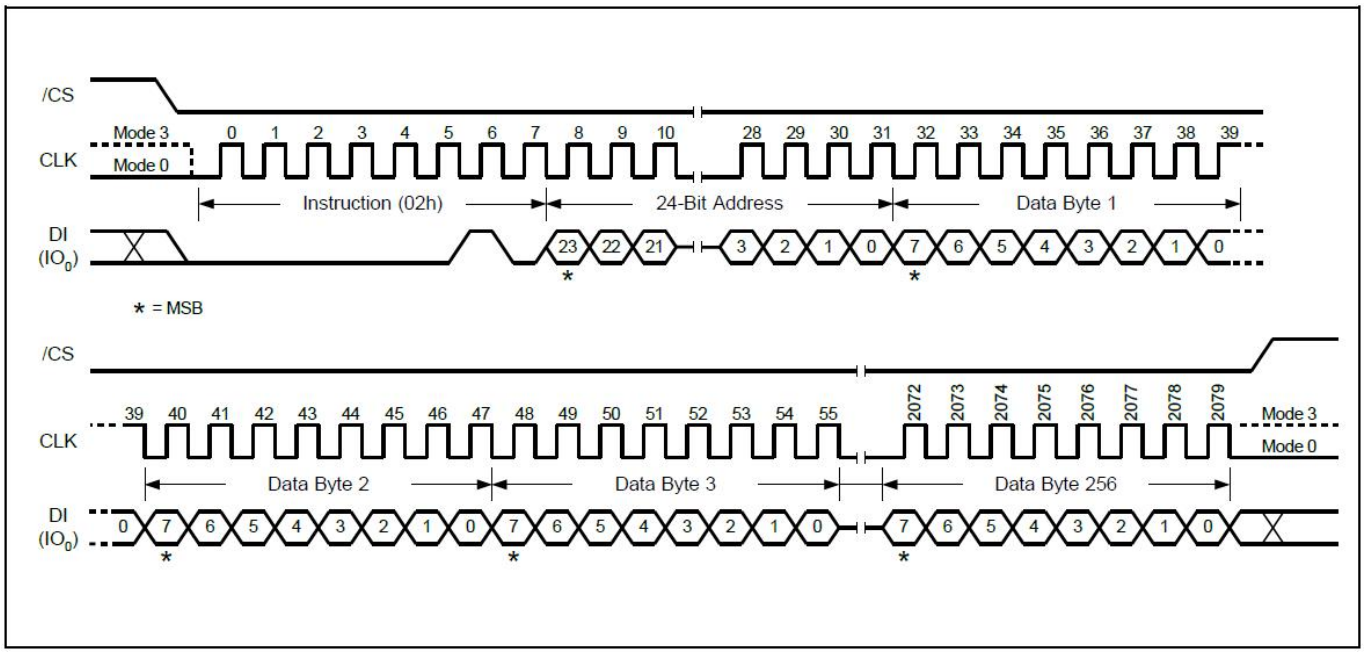



Figure9 Page Program Sequence Diagram

## 9.12 Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen 4KB sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure10. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is Tse) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bit (see Table 1-6) is not executed.

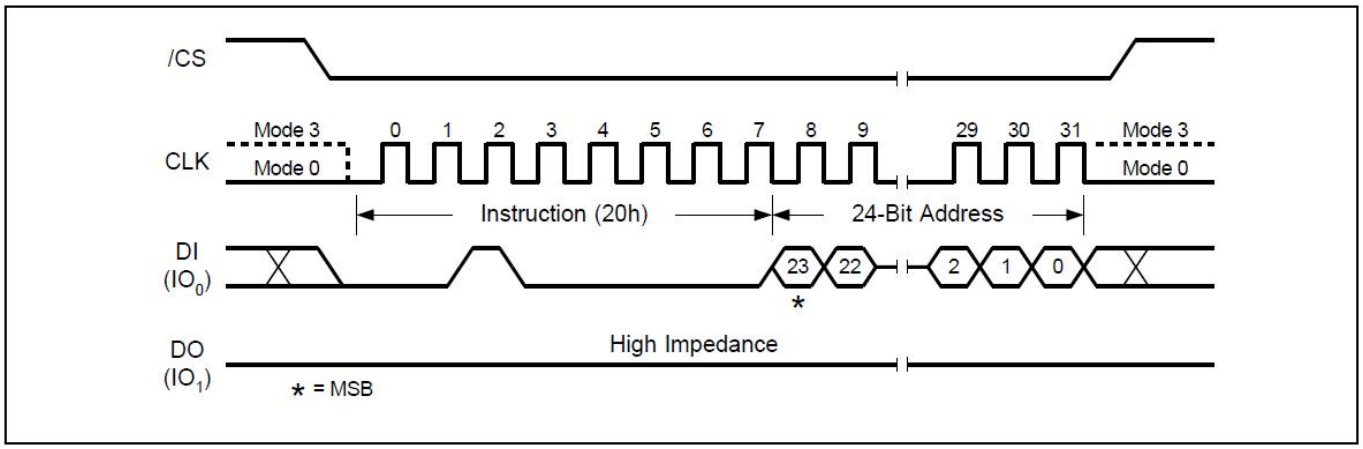



Figure10. Sector Erase Sequence Diagram

## 9.13 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure11. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is Tse) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, and BP0) bits (see Table 1-3) is not executed.

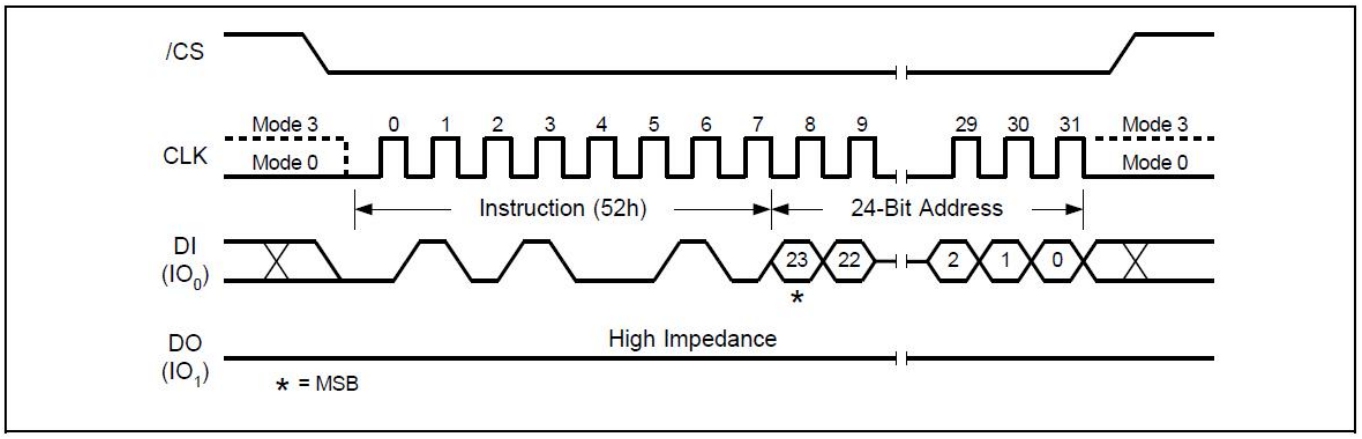



Figure11. 32KB Block Erase Sequence Diagram

## 9.14 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure 12. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is Tse) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, and BP0) bits (see Table 1-3) is not executed.

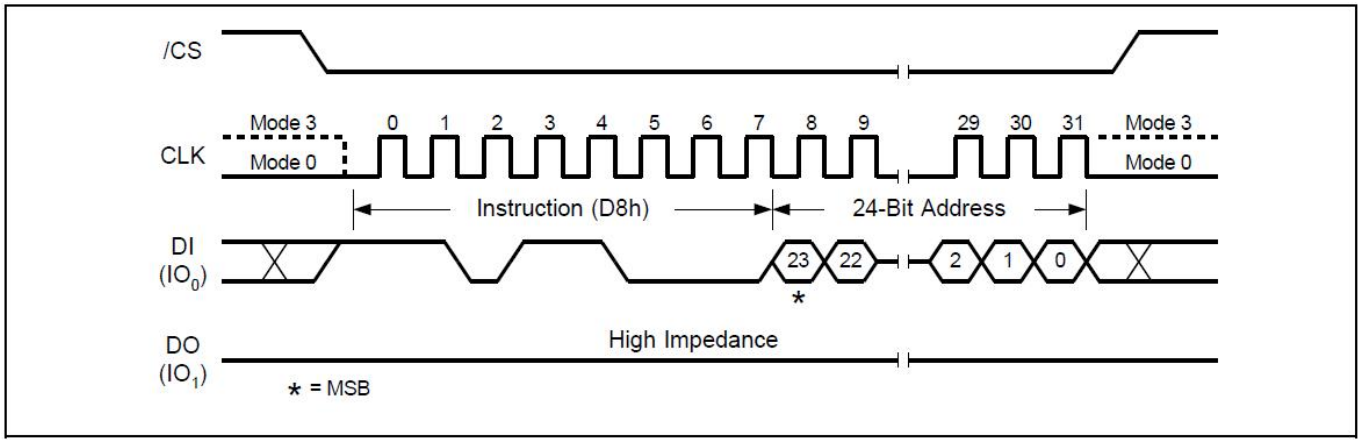



Figure12. 64KB Block Erase Sequence Diagram

## 9.15 Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure13. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is Tce) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0.

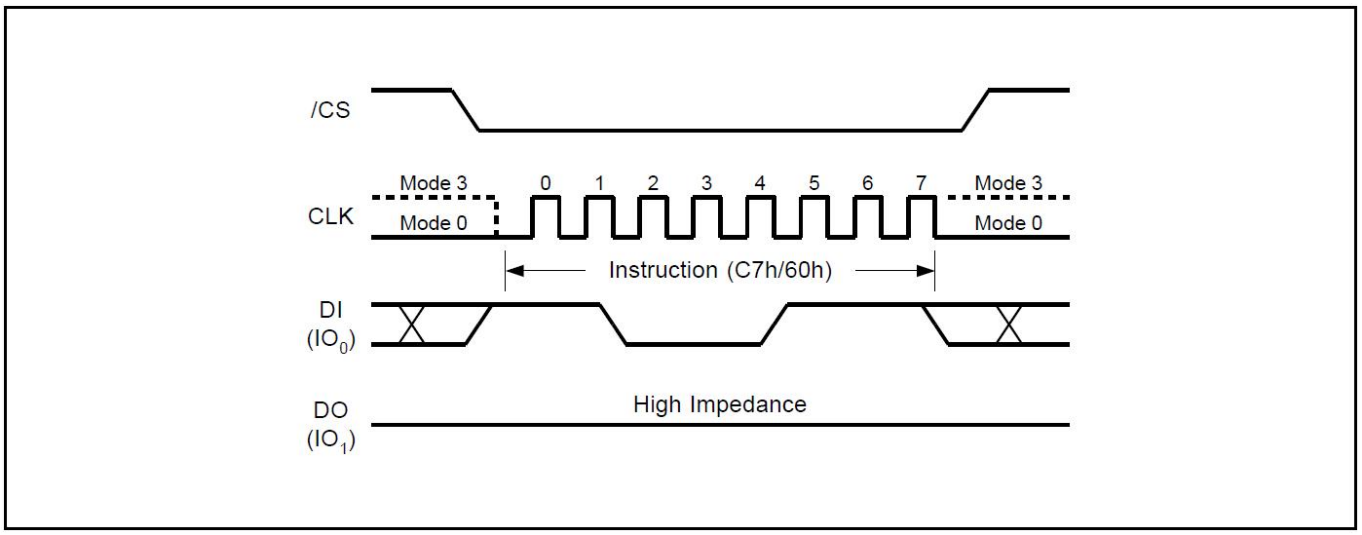



Figure13. Chip Erase Sequence Diagram

## 9.16 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on DO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power- Up. The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure14. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of Tdp before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power- Down (DP) command, while an Erase, Program or Write cycle is in progress.

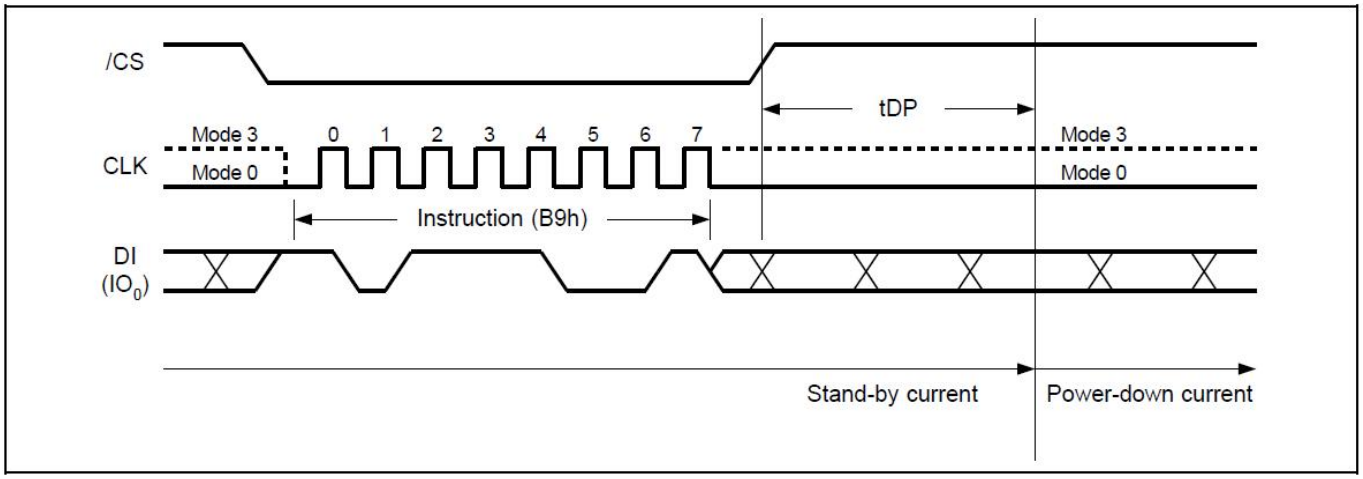



Figure14. Deep Power-Down Sequence Diagram

## 9.17 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure15. Release from Power-Down will take the time duration of Tres1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the Tres1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure15. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure15, except that after CS# is driven high it must remain high for a time duration of Tres2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equal 1) the command is ignored and will not have any effects on the current cycle.

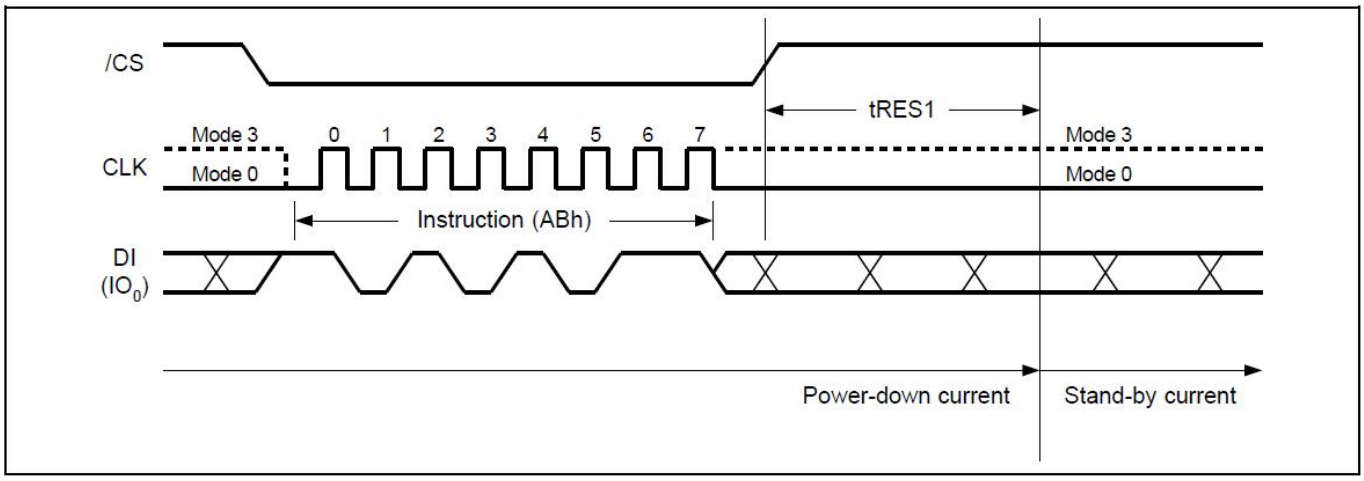



Figure15a. Release Power-Down Sequence Diagram

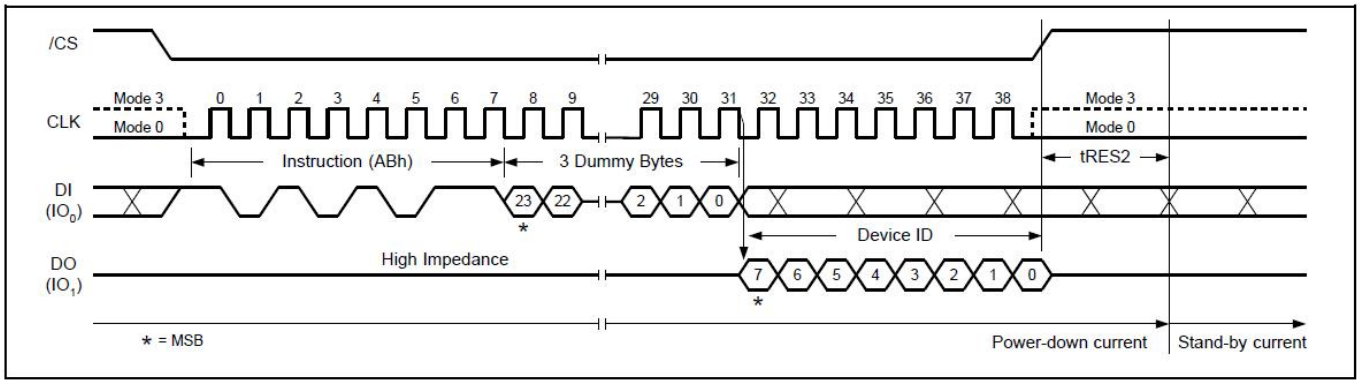



Figure15b. Release Power-Down/Read Device ID Sequence Diagram

## 9.18 Read Manufacture Id/ Device Id (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure16. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

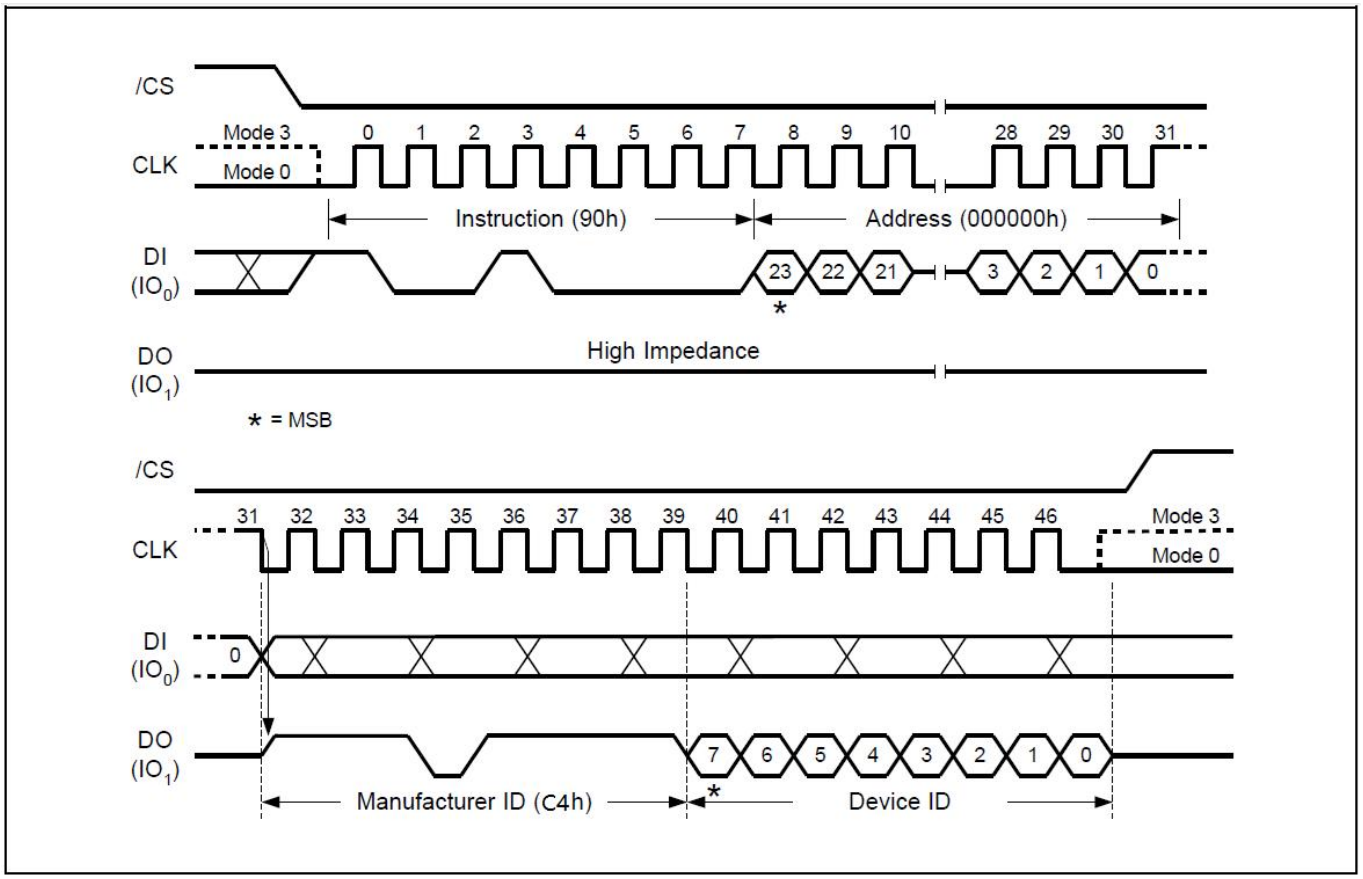



Figure16 Read Manufacture ID/ Device ID Sequence Diagram

## 9.19 Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The command sequence is shown in Figure 17. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

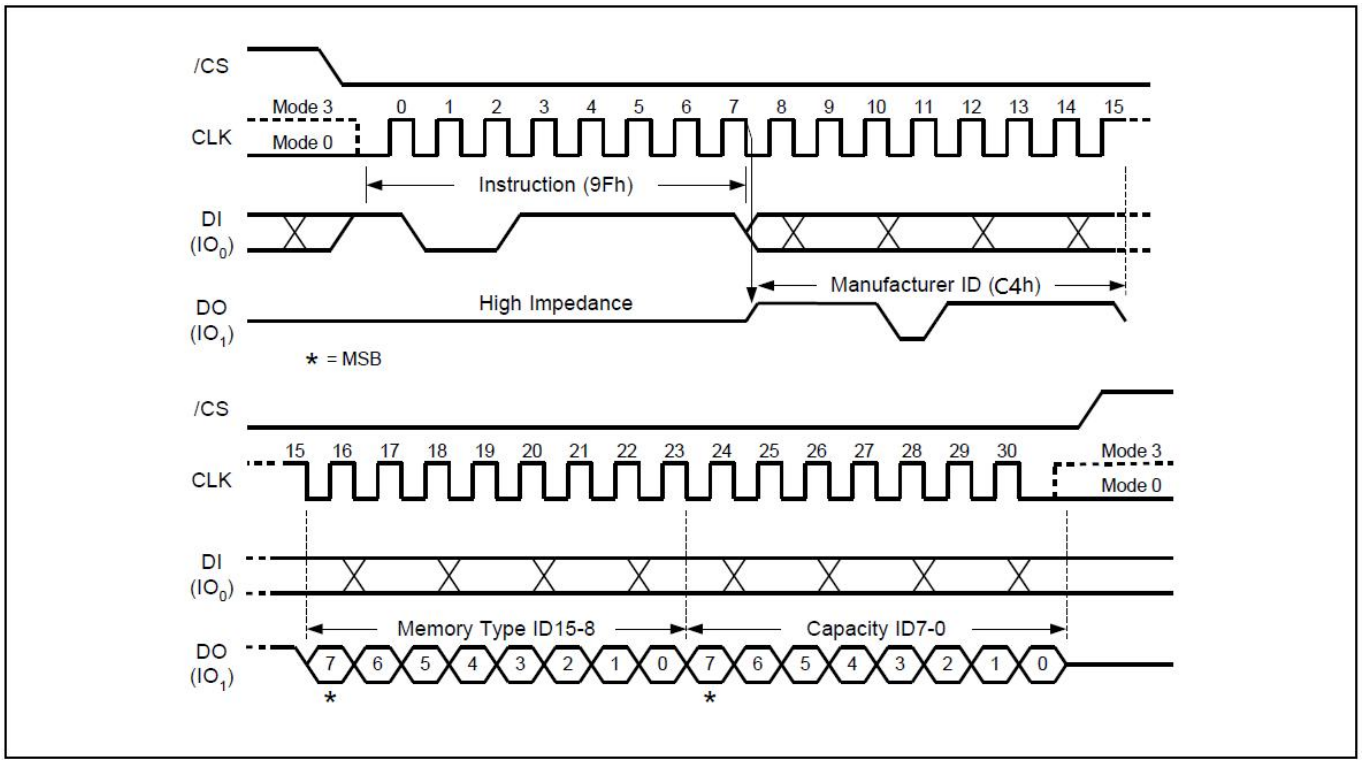



Figure17.Read Identification ID Sequence Diagram

## 9.20 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each GT25D20/10/05E device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in figure 18.

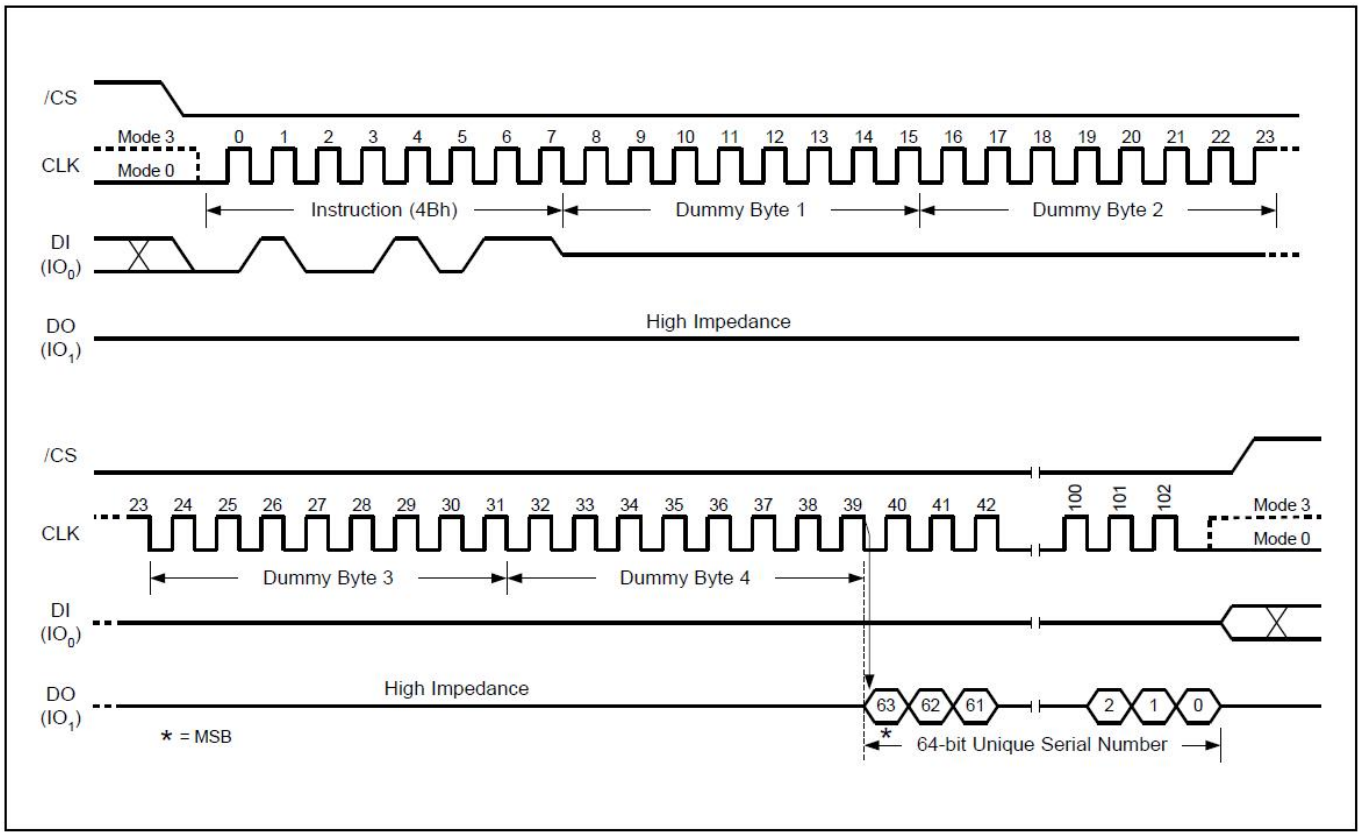



Figure18. Read Unique ID Number Instruction Sequence

## 9.21 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), , Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The "Enable Reset (66H)" and the "Reset (99H)" commands can be issued in either SPI mode. The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately Trst/Trst_E to reset. During this period, no command will be accepted.

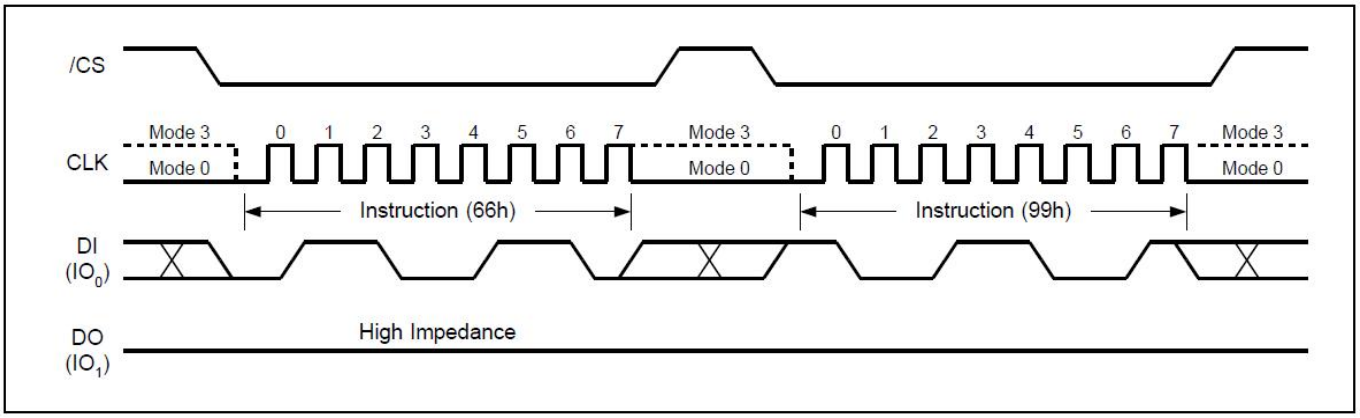
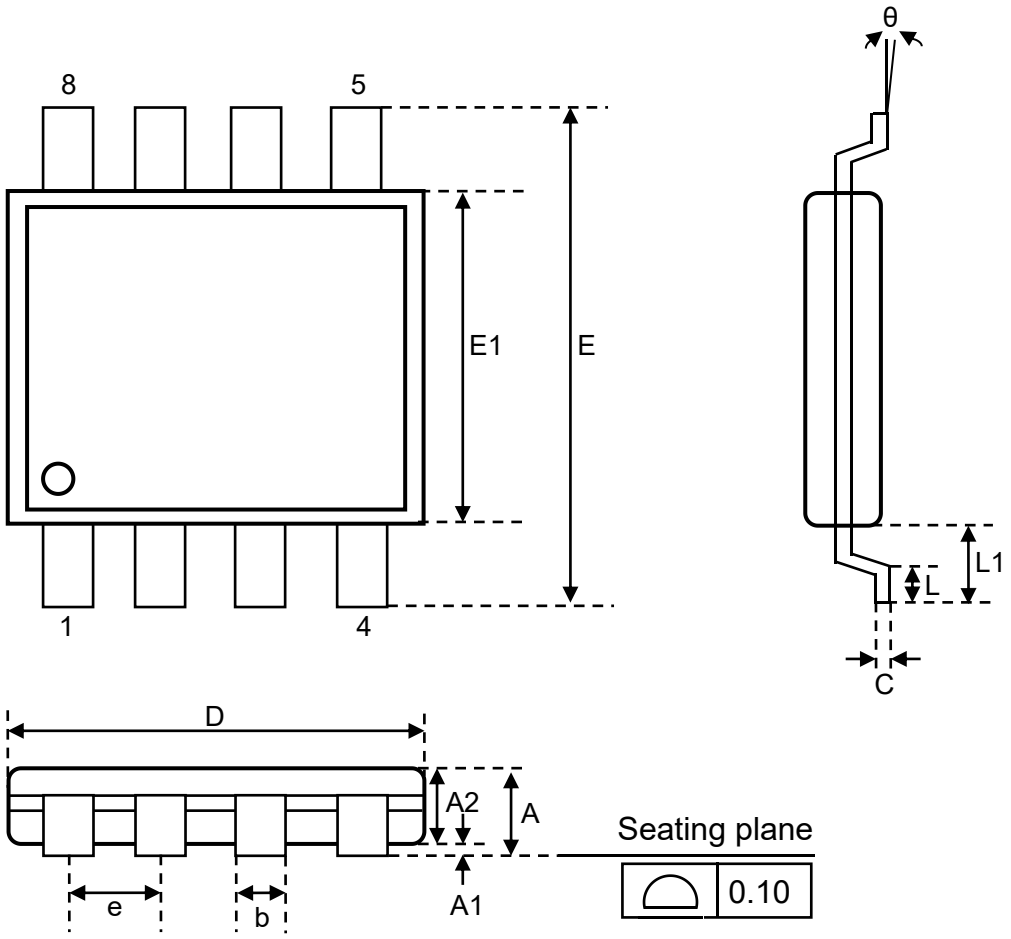



Figure19. Enable Reset and Reset Instruction Sequence

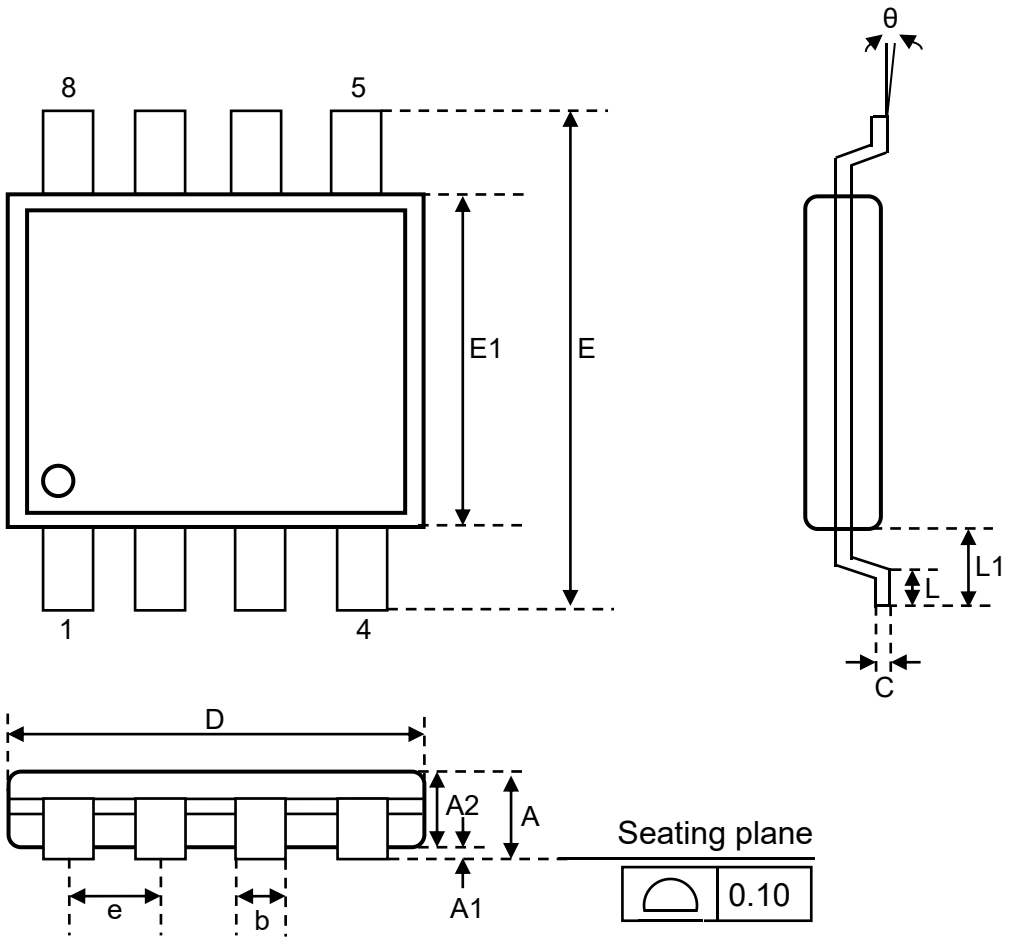
## 10 Package Information

### 10.1 Package SOP8 208MIL



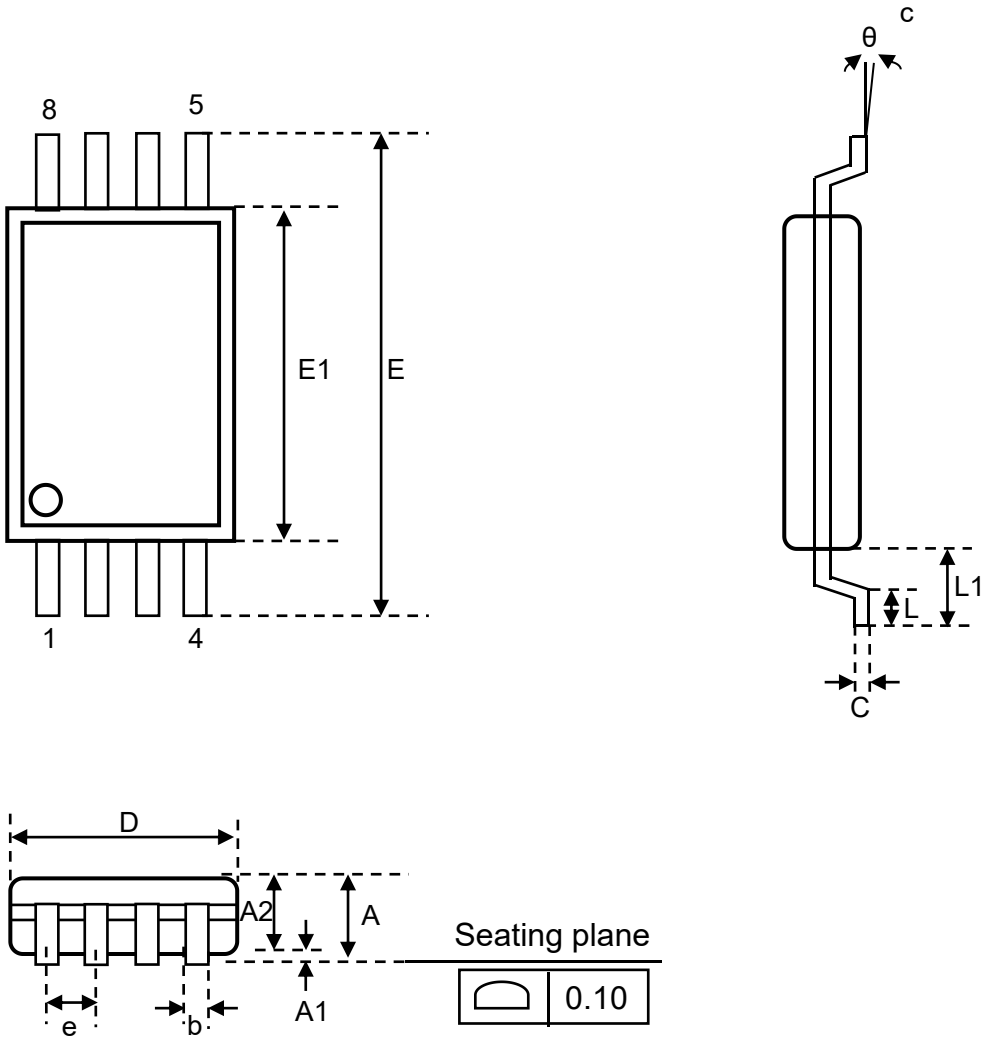

| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.75 | 1.95 | 2.16 | 0.069 | 0.077 | 0.085 |
| A1 | 0.05 | 0.15 | 0.25 | 0.002 | 0.006 | 0.010 |
| A2 | 1.70 | 1.80 | 1.91 | 0.067 | 0.071 | 0.075 |
| b | 0.31 | 0.41 | 0.51 | 0.012 | 0.016 | 0.020 |
| C | 0.18 | 0.21 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 |
| E | 7.70 | 7.90 | 8.10 | 0.303 | 0.311 | 0.319 |
| E1 | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| e | | 1.27 | | | 0.050 | |
| L | 0.50 | 0.67 | 0.85 | 0.020 | 0.026 | 0.033 |
| L1 | 1.21 | 1.31 | 1.41 | 0.048 | 0.052 | 0.056 |
| θ | 0° | 5° | 8° | 0° | 5° | 8° |

## 10.2 Package SOP8 150MIL




| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.35 | - | 1.75 | 0.053 | - | 0.069 |
| A1 | 0.10 | - | 0.25 | 0.004 | - | 0.010 |
| A2 | 1.35 | - | 1.55 | 0.053 | - | 0.061 |
| b | 0.31 | - | 0.51 | 0.012 | 0.016 | 0.020 |
| C | 0.10 | - | 0.25 | 0.004 | - | 0.010 |
| D | 4.80 | 4.90 | 5.03 | 0.189 | 0.193 | 0.197 |
| E | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.80 | 3.90 | 4.00 | 0.149 | 0.154 | 0.158 |
| e | - | 1.27 | - | - | 0.050 | - |
| L | 0.40 | - | 0.90 | 0.016 | - | 0.035 |
| L1 | 0.85 | 1.06 | 1.27 | 0.033 | 0.042 | 0.050 |
| θ | 0° | - | 8° | 0° | - | 8° |

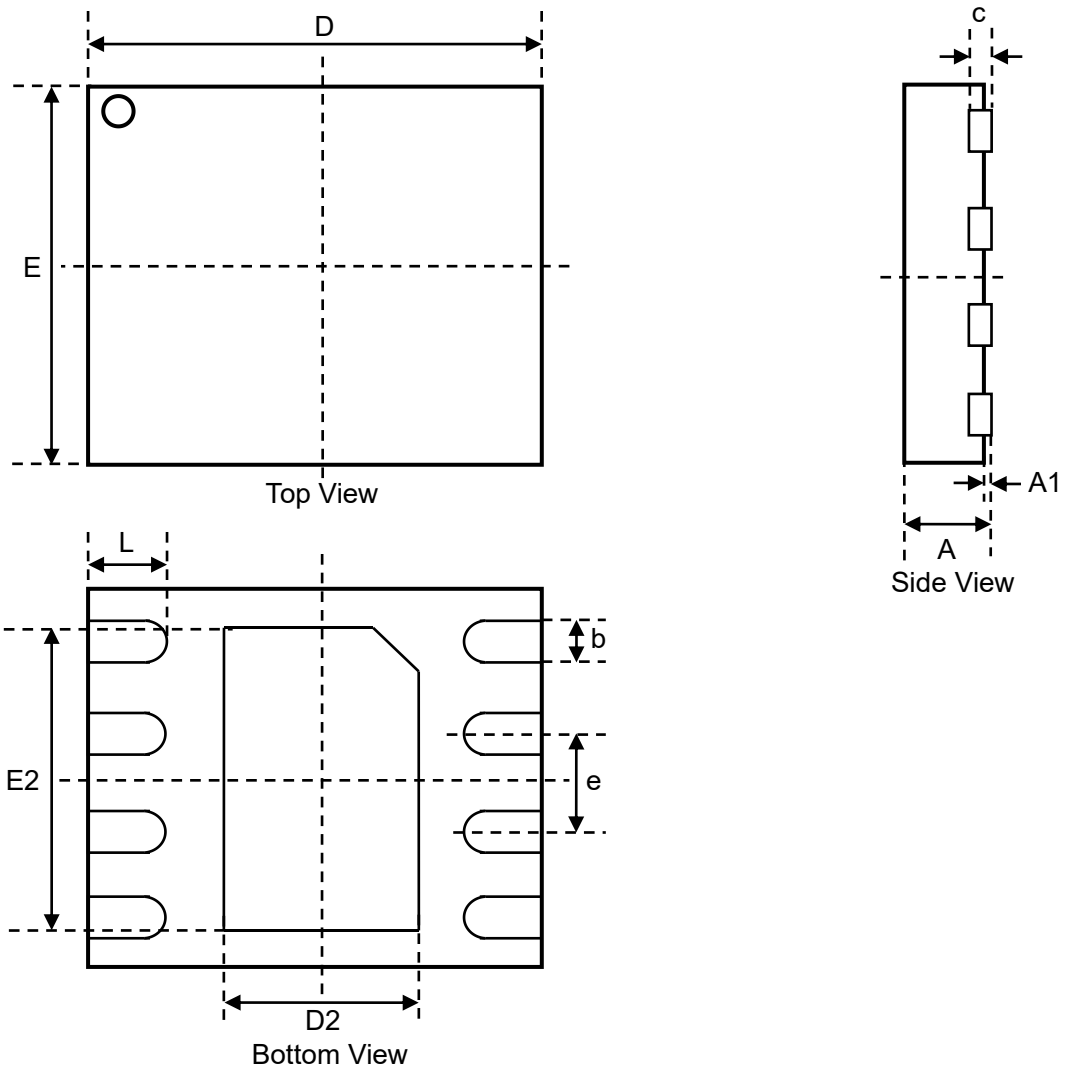
## 10.3 Package TSSOP8L (173mil)




| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 1.20 | - | - | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.112 |
| E | 6.30 | 6.40 | 6.50 | 0.248 | 0.252 | 0.256 |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | - | 0.65 | - | - | 0.026 | - |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 0.85 | 1.00 | 1.15 | 0.033 | 0.039 | 0.045 |
| θ | 0 | 4 | 8 | 0 | 4 | 8 |

Note:
1. The exposed metal pad area on the bottom of the package is floating.

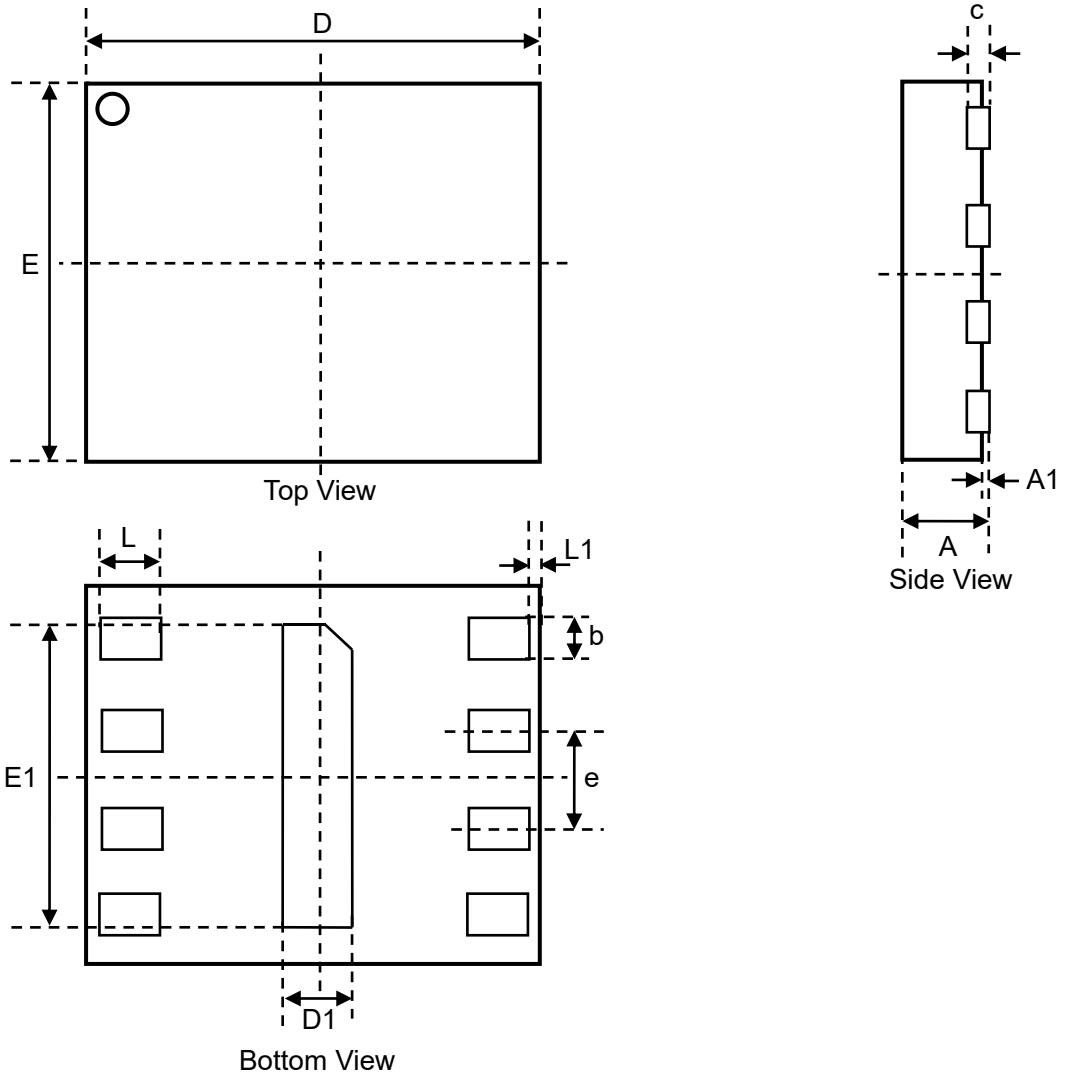
## 10.4 Package WSON8 (6*5mm)




| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| c | 0.180 | 0.203 | 0.250 | 0.007 | 0.008 | 0.010 |
| b | 0.35 | 0.40 | 0.50 | 0.014 | 0.016 | 0.020 |
| D | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| D2 | 3.30 | 3.40 | 3.50 | 0.130 | 0.134 | 0.138 |
| E | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E2 | 3.90 | 4.00 | 4.10 | 0.154 | 0.157 | 0.161 |
| e | | 1.27 | | | 0.05 | |
| L | 0.50 | 0.60 | 0.75 | 0.020 | 0.024 | 0.030 |

Note:
13. The exposed metal pad area on the bottom of the package is floating.

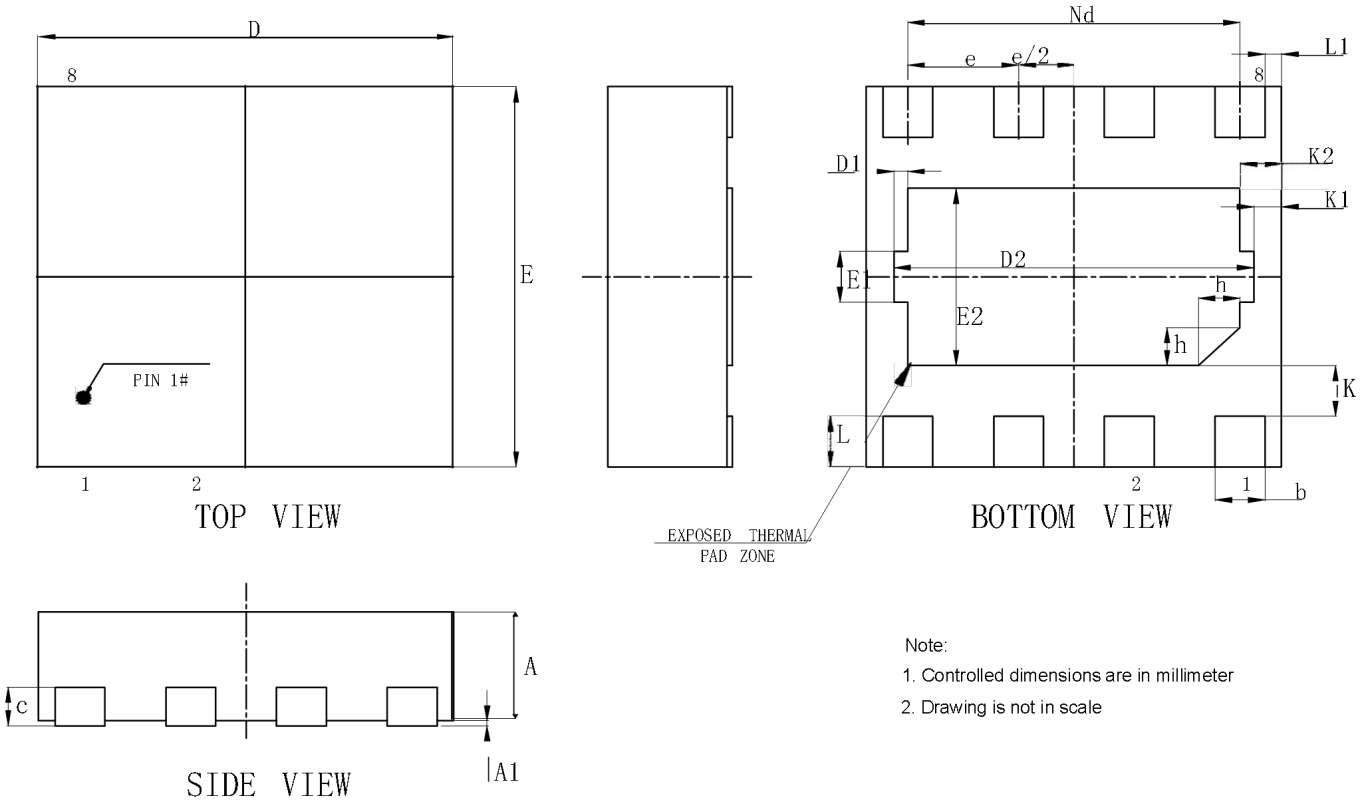
## 10.5 Package USON8 (2*3mm)




| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| A1 | 0.00 | 0.02 | 0.05 | | 0.001 | 0.002 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| D1 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| E | 1.90 | 2.00 | 2.10 | 0.075 | 0.079 | 0.083 |
| E1 | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |
| e | | 0.50 | | | 0.020 | |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| L1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |

Note:
1. The exposed metal pad area on the bottom of the package is floating.

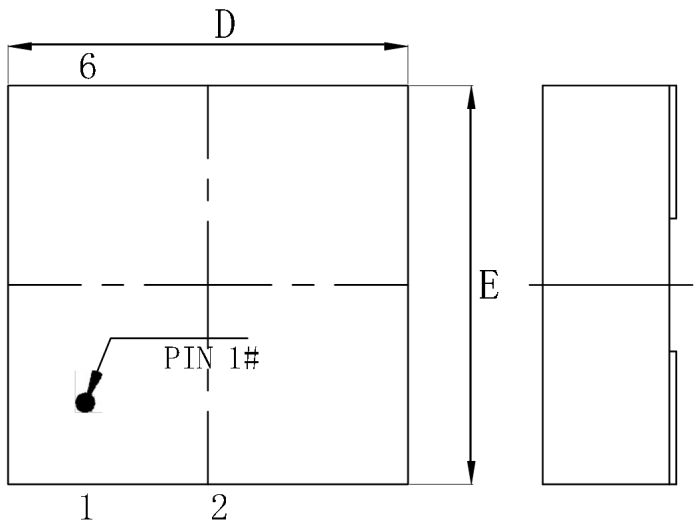
## 10.6 Package 8Pin USON1.5*1.5



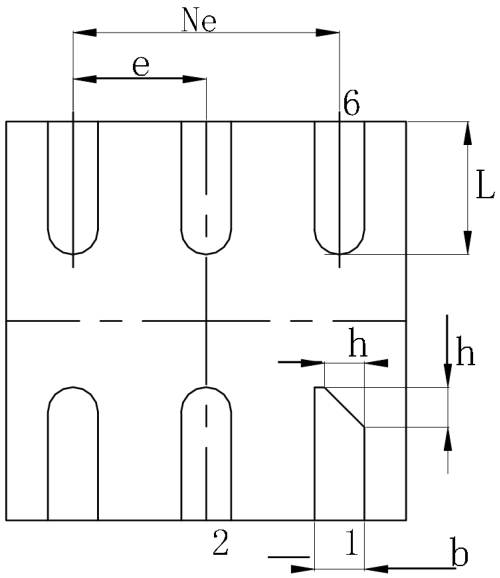

Note:
1. Controlled dimensions are in millimeter
2. Drawing is not in scale

| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.400 | 0.450 | 0.500 | 0.016 | 0.018 | 0.020 |
| A1 | 0.000 | 0.020 | 0.050 | 0.000 | 0.001 | 0.002 |
| b | 0.130 | 0.180 | 0.230 | 0.005 | 0.007 | 0.009 |
| c | | 0.152 | | -- | 0.006 | -- |
| D | 1.450 | 1.500 | 1.550 | 0.057 | 0.059 | 0.061 |
| D1 | | 0.050 | | -- | 0.002 | -- |
| D2 | 1.200 | 1.300 | 1.400 | 0.047 | 0.051 | 0.055 |
| e | | 0.400 | | -- | 0.016 | -- |
| Nd | | 1.200 | | -- | 0.047 | -- |
| E | 1.450 | 1.500 | 1.550 | 0.057 | 0.059 | 0.061 |
| E1 | | 0.200 | | -- | 0.008 | -- |
| E2 | 0.600 | 0.700 | 0.800 | 0.024 | 0.028 | 0.031 |
| L | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| L1 | | 0.060 | | -- | 0.002 | -- |
| K | | 0.200 | | -- | 0.008 | -- |
| K1 | | 0.100 | | -- | 0.004 | -- |
| K2 | | 0.150 | | -- | 0.006 | -- |
| h | 0.100 | 0.150 | 0.200 | 0.004 | 0.006 | 0.008 |

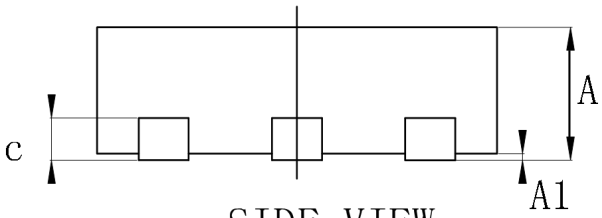
## 10.7 Package 6Pin USON1.2*1.2




TOP VIEW




BOTTOM VIEW

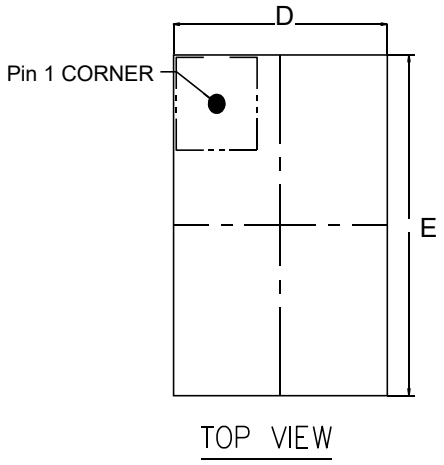


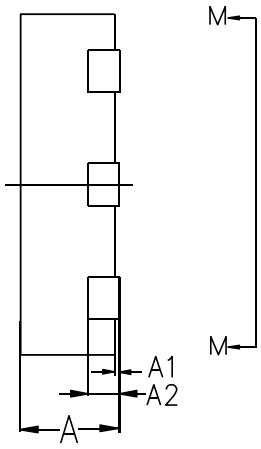

SIDE VIEW

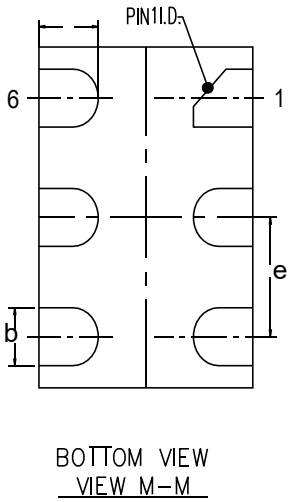
Note:
1. Controlled dimensions are in millimeter
2. Drawing is not in scale

| Symbol | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.320 | - | 0.410 | 0.012 | -- | 0.016 |
| A1 | 0.000 | 0.020 | 0.050 | 0.000 | 0.001 | 0.002 |
| b | 0.100 | 0.150 | 0.200 | 0.004 | 0.006 | 0.008 |
| c | | 0.127 | | -- | 0.005 | -- |
| D | 1.100 | 1.200 | 1.300 | 0.043 | 0.047 | 0.051 |
| e | | 0.400 | | -- | 0.016 | -- |
| Ne | | 0.800 | | -- | 0.031 | -- |
| E | 1.100 | 1.200 | 1.300 | 0.043 | 0.047 | 0.051 |
| L | 0.320 | 0.400 | 0.480 | 0.013 | 0.016 | 0.019 |
| h | | 0.120 | | -- | 0.005 | -- |

## 10.8 Package 6-Land USON 0.72*1.0

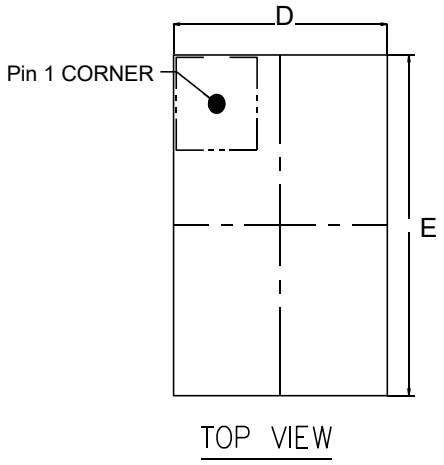


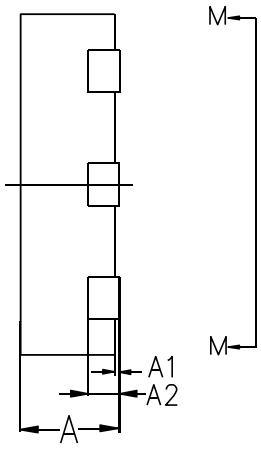



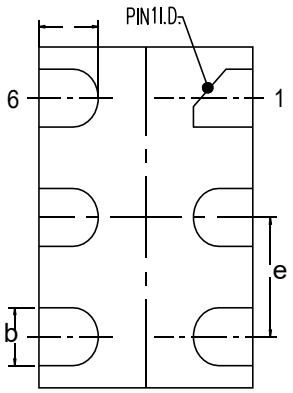




| SYMBOLS | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| A1 | 0.00 | -- | 0.05 | 0.000 | | 0.002 |
| b | 0.14 | 0.17 | 0.2 | | | |
| A2 | 0.127REF | | | 0.005REF | | |
| D | 0.68 | 0.72 | 0.76 | 0.027 | 0.028 | 0.030 |
| E | 0.96 | 1.00 | 1.04 | 0.034 | 0.039 | 0.041 |
| e | 0.35BSC | | | 0.14BSC | | |
| L | 0.17 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |

## 10.9 Package 6-Land USON 0.72*1.1




| SYMBOLS | mm | | | Inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| A1 | 0.00 | -- | 0.05 | 0.000 | | 0.002 |
| b | 0.14 | 0.17 | 0.2 | | | |
| A2 | 0.127REF | | | 0.005REF | | |
| D | 0.68 | 0.72 | 0.76 | 0.027 | 0.028 | 0.030 |
| E | 1.06 | 1.10 | 1.14 | 0.042 | 0.043 | 0.045 |
| e | 0.40BSC | | | 0.016BSC | | |
| L | 0.17 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |

## 11 Ordering Information

GT XXX XX X – X XX X X – XX

### Company

GT=Giantec

### Product Family

25Q = Quad SPI Nor Flash  25D = Dual SPI Nor Flash

### Density

| | | |
|---|---|---|
| 05 = 512Kb | 80=8Mb | 128=128Mb |
| 10 = 1Mb | 16=16Mb | 256=256Mb |
| 20 = 2Mb | 32=32Mb | 512=512Mb |
| 40 = 4Mb | 64=64Mb | |

### Version

E = E Version

### Operation Voltage

U=1.65V ~ 3.6V

### Package Type

W = SOP8 208 mil
G = SOP8 150 mil
Z = TSSOP8 173mil
WS = WSON 6x5 mm
ED = USON 2x3 mm
MD = USON 0.72*1.0mm
LD = USON 0.72*1.1mm
VD = USON 1.5x1.5 mm
TD = USON 1.2x1.2 mm
XKU30 = Sorted and Un-inked KGD

### Green Code

L=Pb Free

### Temperature Range

I = Industrial(-40℃ to +85℃)
IE= Industrial(-40℃ to +105℃)

### Packing

TR= Tape & Reel  Blank = Tube packing

## 12 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the GT25D20/10/05E SPI iFlash Memory. Please contact Giantec for specific availability by density and package type.

| Density | Package Type | Product Number | Top Side Marking Industy(-40℃~85℃) |
|---|---|---|---|
| 2Mb | SOP8 208mil | GT25D20E-UWLI-TR | G YWW 620E-UWLI |
| | SOP8 150mil | GT25D20E-UGLI-TR | G YWW 620E-UGLI |
| | TSSOP 173mil | GT25D20E-UZLI-TR | GT 620E -UZLI YWW |
| | WSON 5x6 | GT25D20E-UWSLI-TR | GT 620E UWSLI YWW |
| | USON 2x3 | GT25D20E-UEDLI-TR | GT 620E YWW |
| | USON 1.5x1.5 | GT25D20E-UVDLI-TR | G2E YWW |
| | USON 1.2x1.2 | GT25D20E-UTDLI-TR | G3 YW |
| | USON 6-Land 0.72*1.0 | GT25D20E-UMDLI-TR | AYW |
| | USON 6-Land 0.72*1.1 | GT25D20E-ULDLI-TR | 1AYW |
| 1Mb | SOP8 208mil | GT25D10E-UWLI-TR | G YWW 610E-UWLI |
| | SOP8 150mil | GT25D10E-UGLI-TR | G YWW 610E-UGLI |
| | TSSOP 173mil | GT25D10E-UZLI-TR | GT 610E -UZLI YWW |
| | WSON 5x6 | GT25D10E-UWSLI-TR | GT 610E UWSLI YWW |
| | USON 2x3 | GT25D10E-UEDLI-TR | GT 610E YWW |
| | USON 1.5x1.5 | GT25D10E-UVDLI-TR | G1E YWW |
| | USON 1.2x1.2 | GT25D10E-UTDLI-TR | G1 YW |
| 512Kb | SOP8 208mil | GT25D05E-UWLI-TR | G YWW 60510E-UWLI |
| | SOP8 150mil | GT25D05E-UGLI-TR | G YWW 605E-UWLI |
| | TSSOP 173mil | GT25D05E-UZLI-TR | GT 605E -UZLI YWW |
| | WSON 5x6 | GT25D05E-UWSLI-TR | GT 605E UWSLI YWW |
| | USON 2x3 | GT25D05E-UEDLI-TR | GT 605E YWW |

## 13 REVISION HISTORY

| Revision | Date | Descriptions |
|---|---|---|
| V1.0 | Jan. 2023 | Initial Version |
| V1.1 | Oct. 2023 | Update status register |
| V1.2 | Dec. 2023 | Update DC&AC |
| V1.3 | Jan. 2024 | Update DC&AC |
| V1.4 | Jun. 2024 | Add USON1.5*1.5 and USON1.2*1.2 |
| V1.5 | Aug. 2024 | Update and add some Top Side Marking |
| V1.6 | Nov. 2024 | Add USON 0.72*1.1 |
| V1.7 | Nov. 2024 | Add 105℃ DC&AC |
| V1.8 | Sep. 2025 | Update Data Retention and AC parameters: Fr, Tshch, Tshqz<br>Some typo correction |
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## Important Notice

Except for customized products which have been expressly identified in the applicable agreement, Giantec's products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and not for use in any applications which may, directly or indirectly, cause death, personal injury, or severe property damages. In the event Giantec products are used in contradicted to their target usage above, the buyer shall take any and all actions to ensure said Giantec's product qualified for its actual use in accordance with the applicable laws and regulations; and Giantec as well as it’s suppliers and/or distributors shall be released from any and all liability arisen therefrom.

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